National Semiconductor®

420521694-001

SuperI/O
PC87351EB
Reference Manual

SuperI/O

PC87351EB

Reference Manual

Part Number: 420521694-001

May 1998

REVISION RECORD

REVISION	RELEASE DATE	SUMMARY OF CHANGES
1.0	March 1998	First release.
1.1	May 1998	Minor Changes.

PREFACE

Thank you for your interest in National Semiconductor's PC87351 SuperI/O device.

The PC87351 Evaluation Board (PC87351EB) is designed to demonstrate the basic I/O functions of the PC87351. It also demonstrates an implementation of the PC87351 on a low chip-count, low-cost PCB.

This Reference Manual provides the information you need to get acquainted with the PC87351, and to develop your own applications.

We at National Semiconductor want you to make the fullest use of your PC87351EB. If you have any questions, please contact your nearest Regional Marketing Office, as listed on the back cover.

PC, PS/2 are registered trademarks of International Business Machines Corporation.

CONTENTS

FIGURES

TABLES

Chapter 1
OVERVIEW

1.1 INTRODUCTION

The PC87351EB is an evaluation board for the PC87351 SuperI/O chip. This chip integrates the traditional I/O devices of a PC motherboard with additional Plug and Play functionality, Infrared, Serial IRQ and Fan support.

The PC87351EB comprises a base board, and an extension board on which the PC87351 SuperI/O chip is mounted.

The PC87351EB enables you to evaluate the following functions, or modules, of the PC87351 in their natural environment:

- ISA interface
- PC87351 external connections
- PC87351 hardware configuration
- Floppy Disk Controller (FDC), up to 1 MB/sec
- 16550 serial port 1
- Enhanced serial port 2, software compatible with 16550
- Infrared (IR) port (supporting IrDA, Sharp, TV Remote)
- Parallel Port, IEEE 1284 compatible (including ECP/EPP)
- Keyboard Controller (KBC) compatible with 8042
- PS/2 mouse and PS/2 keyboard support
- Two General Purpose I/O (GPIO) ports. GPIO1 with 8 bits, and GPIO2 with 3 bits
- System wake-up events detection for energy-saving system
- Two fan speed controls
- Motherboard Plug and Play interface
- V_{SB} standby power pin to minimize battery drainage

Certain features of the PC87351 chip are not supported directly on-board. Figure 2-1 shows the working environment.

Advanced Chip Features

The PC87351 chip supports some of the newest emerging standards in the PC world:

- The Plug and Play standard, driven by Microsoft and Intel, allows a Plug and Play BIOS, or an operating system, to automatically configure and resolve conflicts of I/O addresses, IRQs and DMA channels between ISA boards.

- The TV Remote standard enables you to support applications that either send signals to external devices, or receive signals from remote controls.

1.2 MANUAL ORGANIZATION

This manual provides information for configuring the PC87351EB. It is organized as follows:

Chapter 1 OVERVIEW - Describes the PC87351EB operating environment and features.

Chapter 2 INSTALLATION AND CONFIGURATION - Describes the system installation and configuration procedures.

Chapter 3 THEORY OF OPERATION - Provides a detailed description of the PC87351EB modules, and describes operating principles, based on the schematics in Appendix A.

Chapter 4 SPECIFICATIONS - Provides PC87351EB specifications and physical dimensions.

Appendix A BASE BOARD SCHEMATICS.

Appendix B EXTENSION BOARD SCHEMATICS.

Appendix C BILL OF MATERIALS.

Appendix D PAL EQUATIONS.

1.3 BOARD FEATURES

The PC87351EB includes the following features (see Figure 1-1):

- 128-pin PC87351 SuperI/O Chip
  This device is assembled in a socket for easier upgrade and/or replacement.
- Clock Source
  48 MHz external clock oscillator.
- Two Data Switches
  74LVX3L384 data switches control the data flow from the PC87351 data bus to the X-Bus, or the ISA bus.
- Serial Ports 1 and 2
  Each serial port has a 10-pin dual-row header and a low-cost RS-232 chip (three drivers and five receivers), DS14185.
- Infrared Support
  A 9-pin D-type connector connects the infrared module of the PC87351 to an Infrared Front End Device (IRFE, National Semiconductor discrete module).
- Parallel Port
  A standard D-type male connector with National ECP terminations.
- Floppy Disk Controller (FDC)
  A 34-pin dual-row header connects the FDC block on the PC87351 to a maximum of two external Floppy Disk Drives.

- Keyboard Controller (KBC)
  A 40-pin dual-row header connects the KBC module on the PC87351 to the 8042 40-pin DIP socket on the motherboard. Two MINI-DIN 6-pin connectors connect the mouse and keyboard to the board.

- 3V battery for RAM backup of the PC87351.

- GPIO1
  A 10-pin dual-row header connects all GPIO1 signals to any user-defined external circuitry.

- GPIO2
  A 10-pin dual-row header connects all GPIO2 signals to any user-defined external circuitry.

- PME
  A 10-pin dual-row header connects the multiplexed pins PME1/$\overline{\text{RING}}$ and PME2/$\overline{\text{SUSP}}$ to any user-defined external circuitry.

- FAN
  A 2-pin header connects the fan control to an external fan via optional on-board circuitry.

- Standard AT-type ISA add-on edge connector.

- Voltage Supply
  The board operates at 5V, supplied by the ISA bus. The two DS14185 components, and the fan circuitry on the extension board, operate on +12V and -12V from the ISA bus.

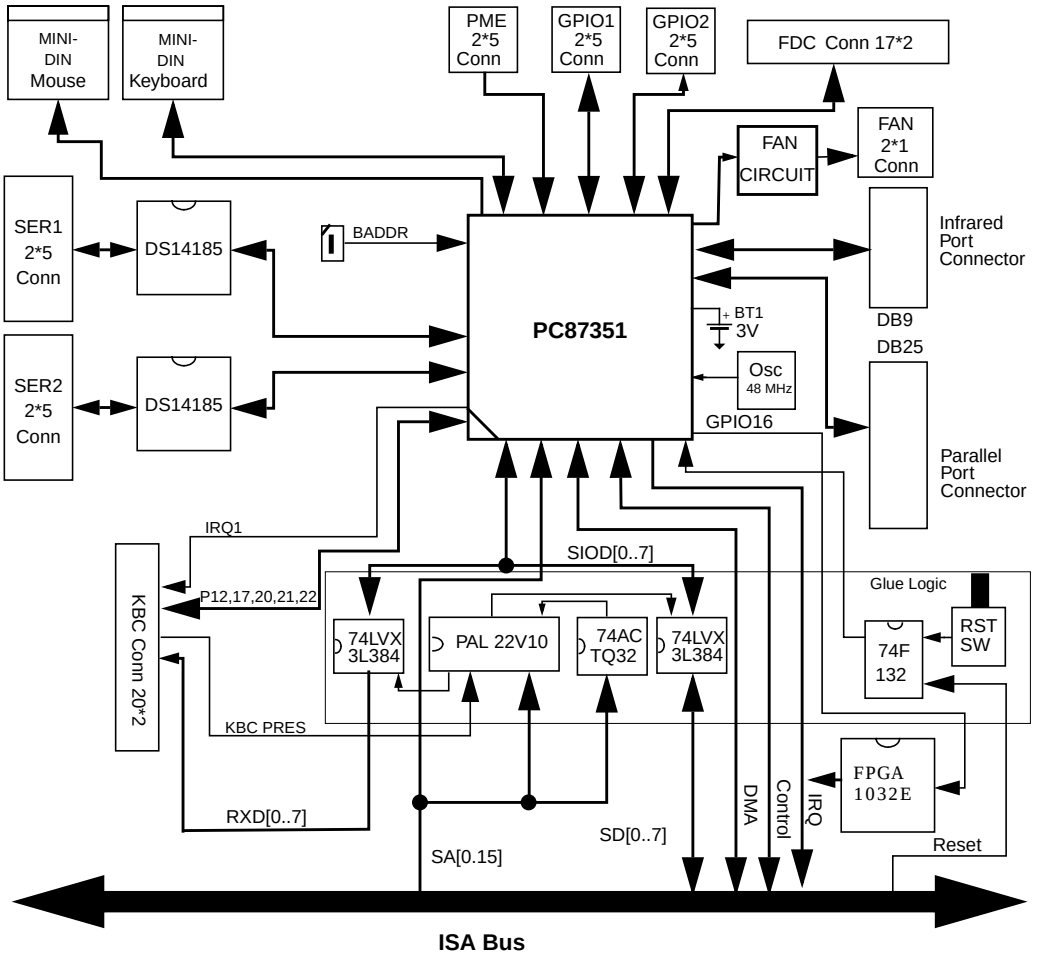


Figure 1-1. PC87351EB Features

1.4 PHYSICAL DESCRIPTION OF BASE BOARD

The PC87351EB is designed to be mounted in a PC-AT slot. Figure 1-2 shows the component side of the base board, and Figure 1-3 the print side.

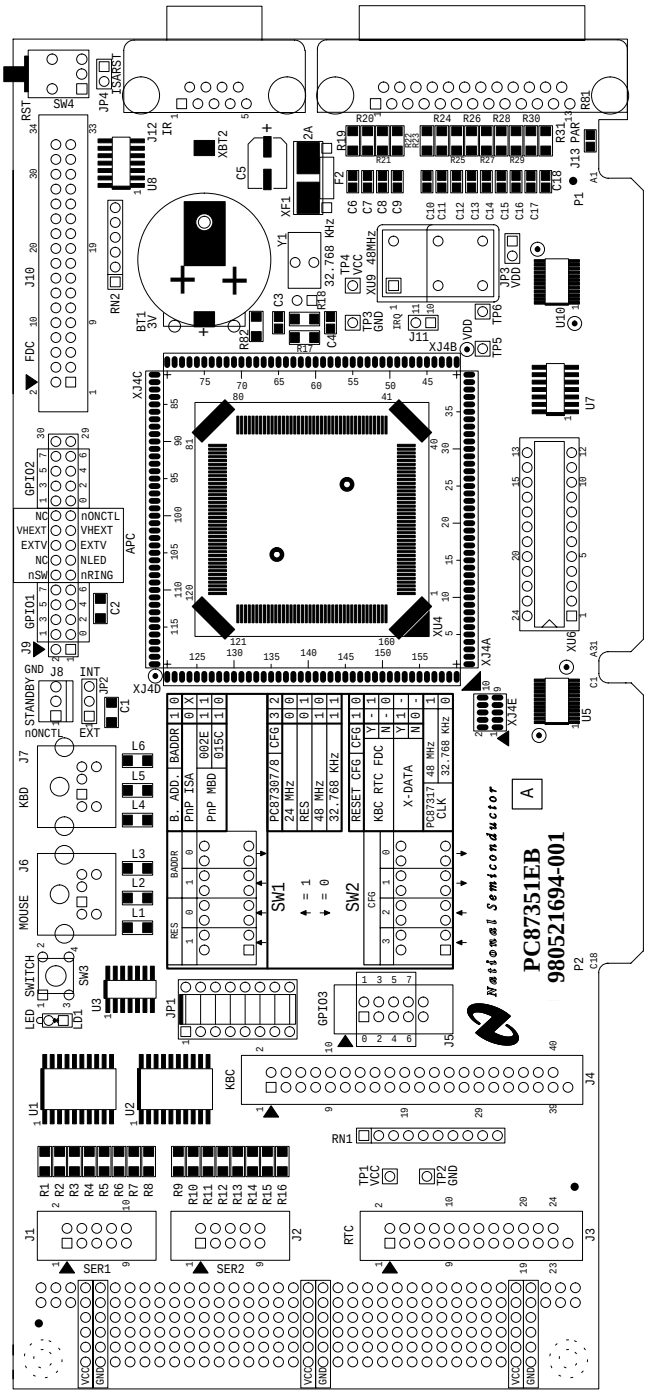


Figure 1-2. PC87351EB Base Board Component-Side Layout

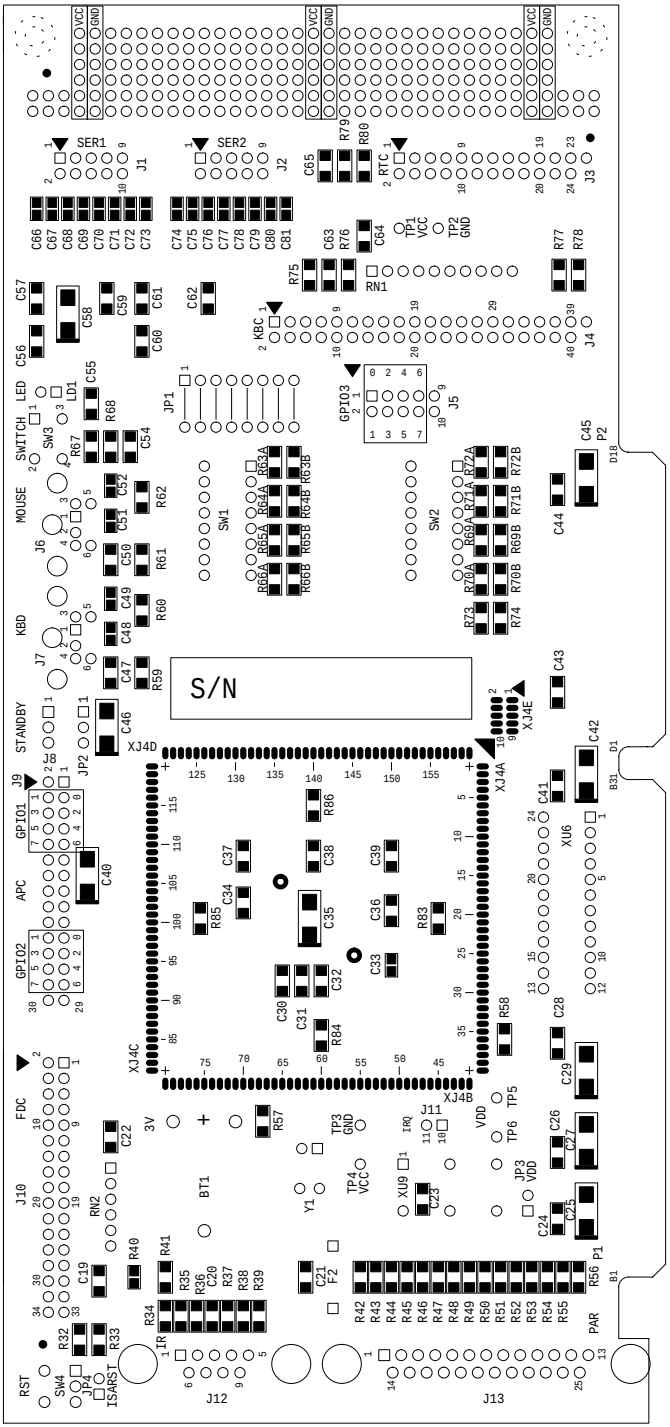


Figure 1-3. PC87351EB Base Board Print-Side Layout

1.5 PHYSICAL DESCRIPTION OF EXTENSION BOARD

The PC87351EB is designed to be mounted in a PC-AT slot. Figure 1-4 shows the component side of the extension board, and Figure 1-5 the print side.

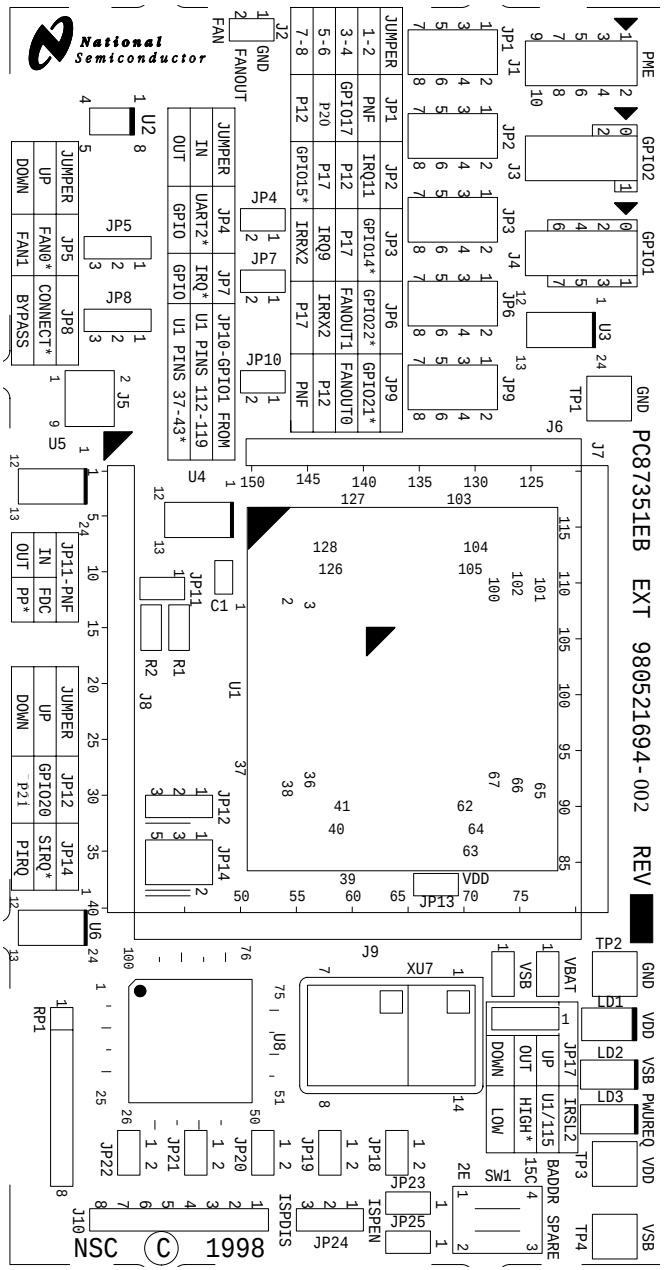


Figure 1-4. PC87351EB Extension Board Component-Side Layout

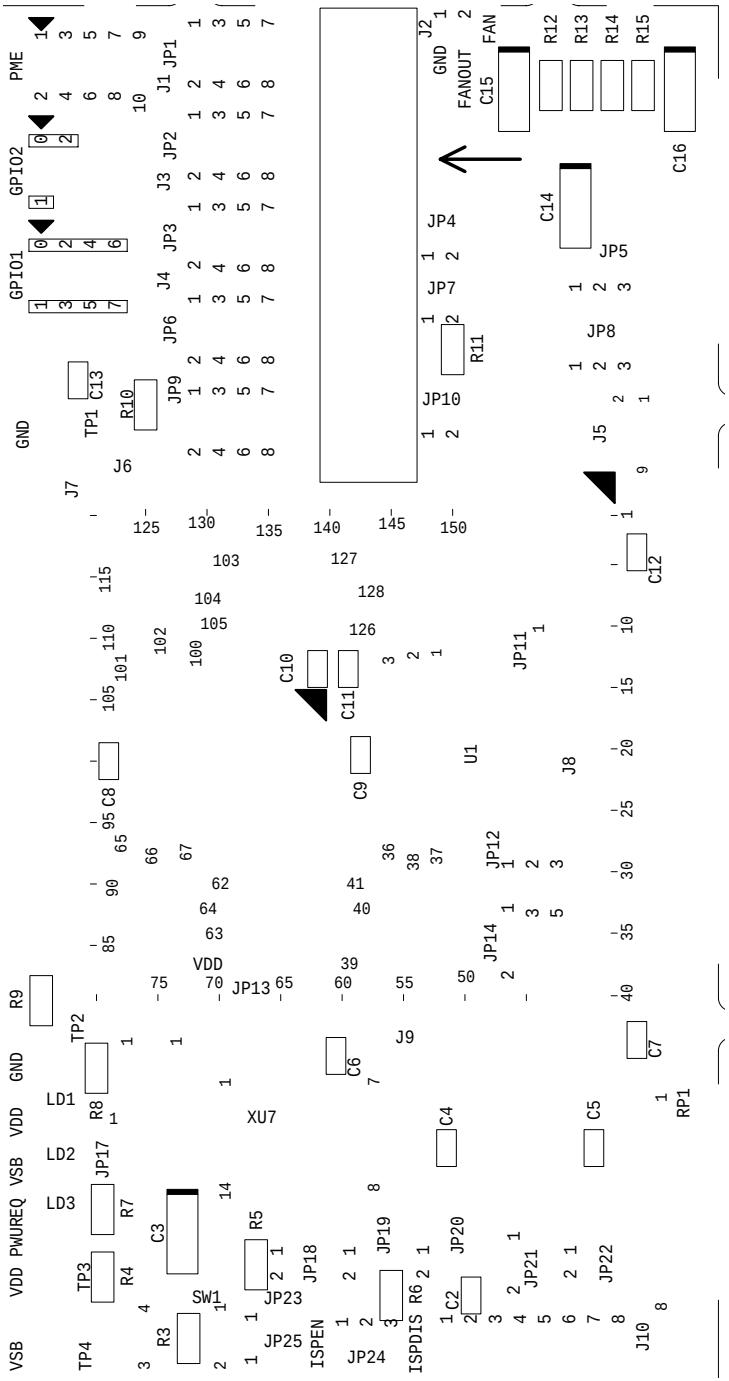


Figure 1-5. PC87351EB Extension Board Print-Side Layout

Chapter 2
INSTALLATION AND CONFIGURATION

2.1 INTRODUCTION

The PC87351EB is an ISA add-in board for a desktop personal computer (PC). The board consists of two parts, a base board and an extension board containing the PC87351 socket. The board can be connected to various external components, including: serial or PS/2 mouse, modem, keyboard, fan, Floppy Disk Drive (FDD), National Semiconductor's Infrared Analog Front End (IRFE) module, printer, GPIO lines and wake-up events lines. Figure 2-1 shows the full PC87351 chip evaluation system.

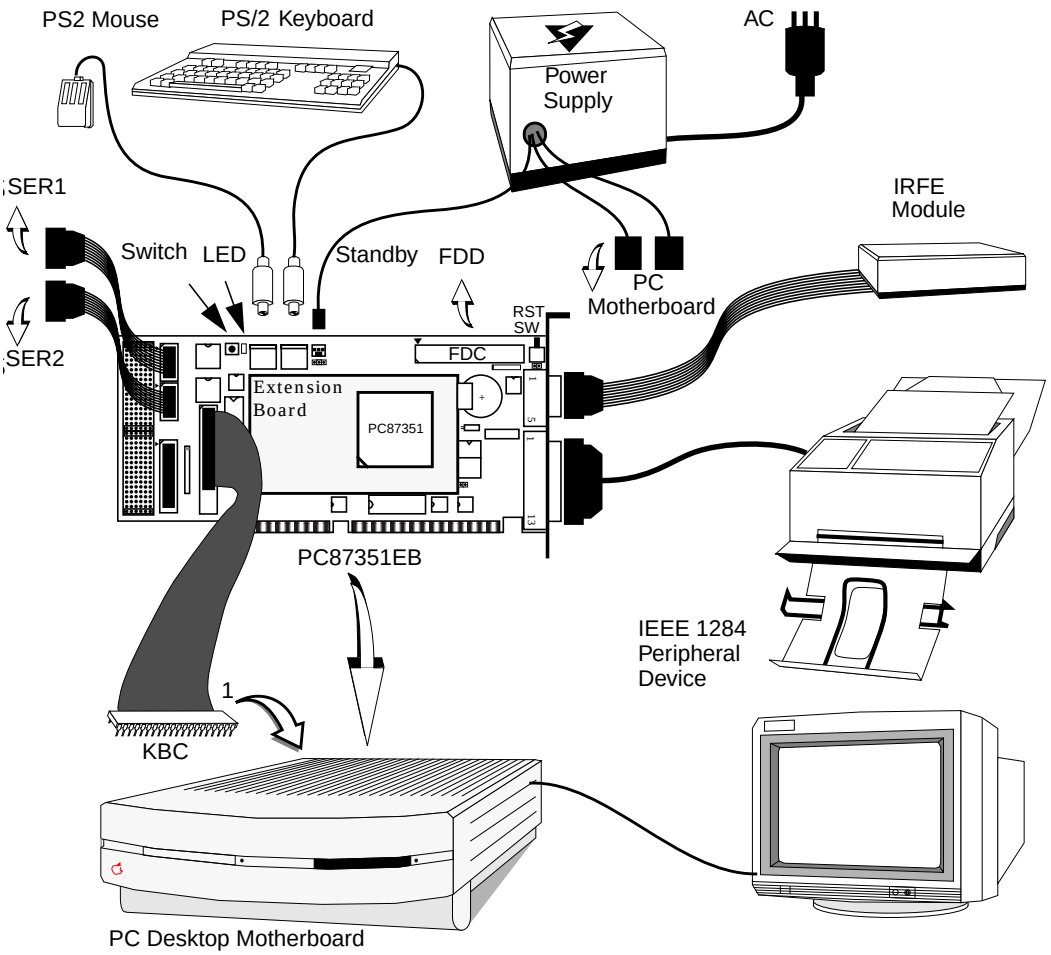


Figure 2-1. PC87351 Chip Evaluation System

2.2 UNPACKING

Verify that your PC87351EB package contains the following items[1]:

1. One PC87351EB (both base board and extension board).

2. One 3.5" floppy disk containing the **`easyreg`** configuration program.

3. One 3.5" floppy disk containing the **`FanDemo`** program.

4. *PC87351 Datasheet.*

5. Two Application Notes:
   Using the SuperI/O PC87351 for Fan Speed Control
   External Circuit Support for Fan Speed Control.

6. This Reference Manual.

7. *PC87351EB Release Letter.*

8. One IRFE module and documentation.

9. One KBC cable.

10. Two IDC10 to DB9 cable adapters for the serial ports.

If any item is missing or damaged, contact your nearest Regional Marketing Office, listed on the back cover of this manual.

2.3 SYSTEM REQUIREMENTS

To fully evaluate the PC87351EB, you need the following equipment:

1. Desktop PC

   The PC87351 chip is evaluated on the PC87351EB via a PC-based evaluation system. The PC87351EB is installed in an ISA bus slot on the PC motherboard.

   To evaluate the KBC module of the PC87351, the motherboard must have a discrete KBC chip in the DIP socket (DIP40), and you must connect the KBC cable from the PC87351 Base Board.

2. PS/2 Keyboard and Mouse

   Connect the keyboard and mouse to the J7 and J6 connectors, respectively, on the PC87351EB base board. Do not connect or disconnect PS/2 peripherals while system power is on.

---

1. The contents may vary according to the release. See the Release Letter for details.

Note Due to keyboard controller ROM code dependency, the PS/2 keyboard connector and mouse connectors may be swapped. If your keyboard does not respond, try swapping the keyboard and mouse cables.

3. External RS-232 Compatible Peripheral Device

   This device can be a serial mouse, modem, terminal, PC-to-PC serial connection, etc. The PC87351EB supports up to two RS-232 serial channels via standard connectors. You can connect the devices to any of the two serial headers on the PC87351EB base board.

Note Use *only* the supplied cables (Type 2), to connect RS-232 compatible peripheral devices.
There are two industry standards for an IDC10-to-DB9 cable:

- Type 1 - Connections according to pin numbers
- Type 2 - Connections according to physical pin locations; used most widely on new motherboards.

Using a Type 1 cable interferes with the functionality of the connection on the PC87351EB. For more details, see Appendix A, Sheet 8.

4. IrDA Compatible IRFE Module

   The PC87351EB supports infrared channel communication via the J12 connector on the PC87351EB base board, which interfaces with the IRFE. For more details about the IRFE features, see the *SuperI/O IRFE Reference Manual.*

5. TV IR Remote Control Device (not supplied)

   To activate the infrared functions of the PC87351EB, you need an external infrared emitting and/or receiving device. This device can be any IrDA-compliant system: another PC, notebook computer, or printer with IR support, etc. You may also use a TV IR remote control device from any manufacturer. If the remote control has a 38 KHz carrier frequency, you may be able to use the internal analog demodulator of the IRFE module to increase operating range.

6. External IEEE 1284 Compliant Peripheral Device

   Connect this device (e.g., printer) to the J13 parallel port connector on the PC87351EB base board, using an IEEE 1284 printer cable. Using other types of cable may lower performance.

7. External Floppy Disk Drive (FDD)

   Connect an FDD to the J10 FDD header on the PC87351EB base board.

8. External Fan

   Connect this device to the J1 Fan header on the PC87351EB extension board.

2.4 SYSTEM INSTALLATION

To install your PC87351EB system, follow the step-by-step procedure below.

Note If you use the KBC, start with the software configuration, Section 2.6.1.

Warning To prevent damage, turn off the PC power supply before you start.

1. Verify the following PC87351EB settings:
   a. Check that all jumpers are in their default positions, (see Tables 2-1 and 2-2).

Table 2-1. Jumper Default Settings on Base Board

Jumper	Default Setting
JP2	1-2 (INT)
JP4	IN

Table 2-2. Jumper Default Settings on Extension Board

Jumper	Default Setting
JP1	5-6 (P20)
JP2	7-8 (GPIO15)
JP3	1-2 (GPIO14)
JP4	IN (UART2)
JP5	UP (FAN0)
JP6	1-2 (GPIO22)
JP7	IN (IRQ)
JP8	UP (CONNECT)
JP9	1-2 (GPIO21)
JP10	OUT (U1 PINS 37-43)
JP11	OUT (P.P.)
JP12	DOWN (P21)
JP13	IN
JP14	DOWN (PIRQ) (Vertical Position)
VBAT	IN
VSB	IN
JP17	OUT (HIGH)
JP18	IN

Table 2-2. Jumper Default Settings on Extension Board (Continued)

Jumper	Default Setting
JP19	IN
JP20	IN
JP21	IN
JP22	IN
JP23	IN
JP24	UP (ISPEN)
JP25	IN

b. Set DIP Switch 1 according to the chip's base address.

2. Install the PC87351EB in an empty ISA slot on the PC motherboard.

3. Connect all peripherals to the appropriate connectors on the PC87351EB. Verify the polarity of all connectors, as shown in Figure 2-1.

Caution Incorrect connections may cause irreversible damage to both the PC87351EB and motherboard. Pay particular attention to the KBC connections.

4. Turn the PC power supply on.

2.5 HARDWARE CONFIGURATION

This section describes the settings of the DIP switch and jumpers, as well as the KBC cable connection.

Note To set up the PC87351EB for a specific application, you must set the DIP switch for the required base address, and the jumpers for the required configuration (Section 2.5.1), and program the PC87351 configuration registers (Section 2.6). For further details, see the *PC87351 Datasheet*.

2.5.1 DIP Switch Setup

A DIP switch on the Extension Board, SW1, enables you to configure the PC87351 base address. The BADDR (Base Address) pin of the PC87351 is sensed during power-up reset. An external 10 KΩ resistor is recommended to pull this pin to V_{CC}.

Table 2-3. Base Address Configuration

BADDR SW1 Position	Index Address	Data Address	Plug and Play Configuration Type
UP	0x015C R/W	0x015D R/W	PnP motherboard - wake up in Config state
DOWN	0x002E R/W	0x002F R/W	PnP motherboard - wake up in Config state

2.5.2 Base Board Jumper Setup

Two base board jumpers (JP2 and JP4) and 25 extension board jumpers (JP1 to JP25) enable you to customize the PC87351EB to your needs.

For details on the base board jumpers, see Appendix A Sheet 4.

JP2

JP2 is located near the STANDBY connector, J8. It selects the source for the chip standby power pin, V_{SB}.

JP2	Description
1-2 (INT, default)	On-board V_{CC}
2-3 (EXT)	Off-board J8

JP4

JP4 is located near the manual reset switch, (SW4). It enables you to use motherboards that assert the ISA reset signal when you perform a system soft reset (<Ctrl><Alt><Delete>). In its default state, IN, it enables both ISA and manual reset.

If you remove this jumper, the chip does not receive the power-on reset signal from the ISA bus. Before you address any of its registers, press the SW4 reset switch to reset the chip manually. For further details, see Section 2.6.

JP4	Description
IN (default)	ISA reset is connected
OUT	ISA reset is not connected

2.5.3 Extension Board Jumper Setup

For details on the extension board jumpers, see the schematics in Appendix B.

JP1-4, JP6-7, JP9

JP1-4, JP6-7 and JP9 route, or control the routing of, some of the multiplexed pins of the PC87351 chip. The SIOCF2 and SIOCF3 registers, of the PC87351 chip, determine the functions of these pins. For a description of these jumpers settings, and the configuration of the PC87351 registers, see the table below.

To avoid contention, keep to the following rules:

1. Do not use more than one jumper for a function.
2. To change configuration, perform the following steps:
   a. Pull out all the above jumpers.
   b. Configure the SIOCF2 and SIOCF3 registers according to the table below.
   c. Insert the jumpers according to the table below.

Signals	JP1	JP2	JP3	JP4	JP6	JP7	JP9
GPIO10-13 GPIO16				**OUT** SIOCF3, bit 0=0		**OUT** SIOCF2, bit 0=0	
GPIO14			**1-2** SIOCF2, bits 2-1=00 or bits 2-0=011				
GPIO15		**7-8** SIOCF2, bits 4-3=00 or bits 4-3,0 =011					
GPIO17	**3-4** SIOCF2, bits 6-5=00						
GPIO21							**1-2** SIOCF3, bits 2-1=00
GPIO22					**1-2** SIOCF3, bits 4-3=00		

Signals	JP1	JP2	JP3	JP4	JP6	JP7	JP9
IRQ4-7 IRQ12						**IN** SIOCF2, bit 0=1	
IRQ9			**5-6** SIOCF2, bits 2-0=011				
IRQ11		**1-2** SIOCF2, bits 4-3,0 =010					
"Hot Key" (P12)	**7-8** SIOCF2, bits 6-5=10	**3-4** SIOCF2, bits 4-3=10					**5-6** SIOCF3, bits 2-1=10
KBC Lock (P17)		**5-6** SIOCF2, bits 4-3=11	**3-4** SIOCF2, bits 2-1=11		**7-8** SIOCF3, bits 4-3=11		
KBRST (P20)	**5-6** SIOCF2, bits 6-5=01						
PNF (in PPM mode)	**1-2** SIOCF2, bits 6-5 =11						**1-2** SIOCF3, bits 8-7 =11
IRRX2 IRSL0			**7-8** SIOCF2, bits 2-1=10		**5-6** SIOCF3, bits 4-3=10		
FANOUT0							**3-4** SIOCF3, bits 2-1=01
FANOUT1					**3-4** SIOCF3, bits 4-3=01		
UART2				**IN** SIOCF3, bit 0=1			

JP4

JP4 controls the state of the electronic switch U4. This switch routes pins 112-115 and 117-120 of the PC87351 chip to the PC87351EB. Set up JP4 according to SIOCF3 bit 0, which determines the function of these pins.

JP4	SIOCF3, Bit 0	Function (PC8735 Pins 112-115 and 117-120)
IN (Default)	1	UART2
OUT	0	GPIO10-16

Note

To avoid contention when JP10 is IN, make sure that GPIO1 connector (J4 on extension board) is not connected to external signals while JP4 and SIOCF3 bit 0 are configured to UART2 mode, or while configuring JP4 and SIOCF3 bit 0.

JP5

JP5 routes either the FAN0, or FAN1, signal from the PC87351 chip to the FAN connector (J2).

JP5	Selected Fan
UP	FAN0
DOWN	FAN1

JP7

JP7 controls the state of the electronic switch U6. This switch routes pins 37-40 and 43 of the PC87351 chip to the PC87351EB board. JP7 should be setup according to SIOCF2 bit 0 which determines the above pins function. See table below.

JP7	SIOCF2, Bit 0	Function (PC87351 Pins 37-40 and 43)
IN (Default)	1	IRQ4-7,12
OUT	0	GPIO10-13, 16

Note

To avoid contention when JP10 is OUT, make sure that GPIO1 connector (J4 on extension board) is not connected to external signals while JP7 and SIOCF2 bit 0 are configured to IRQ mode, or while configuring JP7 and SIOCF2 bit 0.

JP8

To work with DC fans, the PC87351 chip requires an external circuit to interface with the fan. For a fan that does not need an external circuit, you can connect the fan directly to the PC87351 chip.

JP8	Description
UP	The fan is connected to the Fan Control circuit
DOWN	The fan is connected directly to the PC87351 chip

JP10 JP10 selects one of two groups of pins of the PC87351 chip to connect to the GPIO1 connector (GPIO10-GPIO16).

JP10	Selected Pins of the PC87351
IN	112-115, 117-120
OUT	37-43

JP11 In PPM mode, JP11 indicates to the PC87351 chip the type of device connected to J13 on the base board. Set this jumper as shown below, otherwise results are undefined.

JP11	Type of Device Connected to J13
IN	Floppy Disk
OUT	Parallel Device

JP12 JP12 routes the multiplexed pin 98, of the PC87351 chip, either to the GPIO2 connector (J3 on the extension board) or to the base board. Set this jumper according to the function of this pin, which is determined by SIOCF2, bit 7.

JP12	SIOCF2, bit 7	Function (PC87351 Pin 68)
UP	0	GPIO20
DOWN	1	GA20 (P21)

VDD VDD is used only to measure the chip current, and should always be inserted. Do not power-up the board unless this jumper, or an amperemeter, is connected.

VDD Jumper	Description
IN	Normal operating mode
OUT	Illegal, unless replaced by an amperemeter

JP14 JP14 routes the multiplexed pins 34, 35 of the PC87351 chip. Set the jumper according to SIOCF2 register of the PC351, bit 0, as shown below.

JP14	SIOCF2, Bit 0	PC87351 Pin 34	PC87351 Pin 35	Mode of Operation
UP	0	PCICLK	SERIRQ	SIRQ
DOWN	1	IRQ1	IRQ3	Parallel IRQs

VBAT VBAT is used only to measure battery current to the extension board and should always be inserted.

VBAT Jumper	Description
IN	Normal operating mode
OUT	Illegal, unless replaced by an amperemeter

VSB VSB is used only to measure Stand By voltage current to the extension board, and should always be inserted.

VSB Jumper	Description
IN	Normal operating mode
OUT	Illegal, unless replaced by an amperemeter

JP17 JP17 selects the IRSL2 source, or polarity. IRSL2 selects the IRFE mode of operation.

JP17	IRSL2	Mode of Operation
UP	GPIO13 of PC87351 chip	
OUT	1	TV Remote
DOWN	0	DATA

For more information about the IRFE modes, see the IRFE documentation.

JP18-23, 25 JP18-23, 25 are spare.

JP24 JP24 enables, or disables, the ISP. It is used only for development purposes. Always set this jumper in the high position.

JP24	CPLD Outputs
HIGH	ACTIVE (ISP Enabled)
DOWN	FLOAT (ISP Disable)

2.5.4 KBC Connection to the Motherboard

The KBC module is connected directly to the motherboard via a custom-made flat cable that is supplied with the PC87351EB. See Figure 2-1 and Appendix A, Sheet 13.

To connect the KBC to the 40-pin DIP socket on the motherboard keyboard controller chip:

1. Remove the original 8042 chip (or equivalent) and replace it with a 40-pin DIP socket (not supplied).

2. Connect J4 to the socket using only the 40-pin cable provided.

3. Connect the 40-pin cable:
   Pin 1 (brown) on the narrow connector corresponds to pin 1 of J4 on the base board.
   Pin 1 on the other end of the 40-pin cable, is connected to pin 1 of the DIP socket on the motherboard.

Caution Incorrect connections may cause irreversible damage to your PC87351EB and motherboard.

2.5.5 KBC Automatic Hardware Configuration

The PC87351EB has an automatic hardware configuration capability. Assuming that you have connected the KBC cable correctly and securely (see Figure 2-1), it detects the presence of a cable by sensing the V_{CC} pin of the motherboard KBC socket. This is accomplished by means of a PAL input, KBCPRES. For more details, see Appendix D and to Appendix A, Sheet 4 and Sheet 13.

2.6 SOFTWARE CONFIGURATION

2.6.1 Configuring the PC87351 to Work in Parallel IRQ Mode

The PC87351EB supports Parallel IRQ mode only. The configuration process for this mode depends on whether the KBC is used, or not.

Without the KBC To configure the PC87351 chip for Parallel IRQ mode if you are *not* using the KBC:

From your prompt line run:

```
debug
- o BASE ADDRESS 22
- o BASE ADDRESS+1 a0
```

Where BASE ADDRESS refers to the base address of the chip (either 2E or15C). For more details on the base address, see Table 2-3.

With the KBC If you are using the KBC, perform the following steps *before* the hardware installation (an example follows the explanation):

1. Edit a batch file that includes the following lines:

```
o BASE ADDRESS 23
o BASE ADDRESSS+1 1
o BASE ADDRESS 7
o BASE ADDRESS+1 7
o BASE ADDRESS  60
o BASE ADDRESS+1 GPIO1_HIGH_ADDRESS
o BASE ADDRESS 61
o BASE ADDRESS+1 GPIO1_LOW_ADDRESS
o BASE ADDRESS 30
o BASE ADDRESS+1 1
o BASE ADDRESS f0
o BASE ADDRESS+1 16
o BASE ADDRESS f1
o BASE ADDRESS+1 5
o GPIO1_ADDRESS 0
o BASE ADDRESS 22
o BASE ADDRESS+1 a0
q
```

`GPIO1_HIGH_ADDRESS`	refers to the MSB of the GPIO1 address.
`GPIO1_LOW_ADDRESS`	refers to the LSB of the GPIO1 address.
`GPIO1_ADDRESS`	refers to the GPIO1 address which consists of `GPIO1_HIGH_ADDRESS` and `GPIO1_LOW_ADDRESS`.

2. At the beginning of your `autoexec.bat` file, add the following line:

```
debug < [path]/file_name
```

Example The PC87351 chip base address is 15C, and the GPIO1 address is configured to 200h. The batch file, `351config.bat`, is in the root directory.

The first line of the `autoexec.bat` file is:

```
debug < 351config.bat
```

The `351config.bat` file is:

```
o 15c 23
o 15d 1
o 15c 7
o 15d 7
o 15c 60
o 15d 2
o 15c 61
o 15d 0
o 15c 30
o 15d 1
o 15c f0
o 15d 16
o 15c f1
```

```
o 15d 5
o 200 0
o 15c 22
o 15d a0
q
```

2.6.2 Easyreg Software Utility

The advanced features of the PC87351 chip are enabled by software configuration. To facilitate this task, use the `easyreg` software utility supplied with this package.

The `easyreg` Configuration Program is a DOS utility that enables you to view and configure the major features of the chip, in particular the Enhanced UART, and Plug and Play features. `Easyreg` is a stand-alone, executable DOS file (`easyreg.exe`). For a detailed description, see the `README` file on your floppy disk.

2.6.3 PC87351 Reset

The chip must exit the reset cycle prior to accessing its registers. The reset is performed automatically during each powerup, if the JP4 jumper on the base board is inserted (default). If not, you must manually reset the chip by pressing the on-board reset switch, SW4, located near the bracket. After reset, you can override the hardware configuration by programming the configuration registers.

2.6.4 Configuration Register Access

In the Configuration state, the PC87351 Index and Data registers are determined by the BADDR strap option (see Table 2-3). The location of the PC87351 register set complies with the *Plug and Play ISA Specification, Version 1.0a*.

For more details, see the *ISA Plug and Play Specifications, Rev. 1.0a*. For detailed information on accessing the registers of the PC87351, see the *PC87351 Datasheet*.

Chapter 3
THEORY OF OPERATION

3.1 INTRODUCTION

This chapter describes the operation of the main circuit blocks of the PC87351EB, based on the schematics in Appendix A and Appendix B.

See Appendix A, Sheet 1, and Appendix B, Sheet 1, to verify if the revision numbers on your base and extension boards match those of the schematics. If your board is a newer revision, contact your nearest National Semiconductor representative for updated schematics. See the block diagram in Appendix A (Sheet 2) for a root-level representation of the base board design. This will help you locate the various modules described in this chapter.

Note Unless specified otherwise, all component references are to the components on the base board.

3.2 STANDARD ISA BUS ADD-ON CONNECTOR

See Appendix A, Sheet 3 for a diagram of this connector.

This connector includes the AT gold-plated finger sub-connectors, P1 and P2. The connector layout corresponds to an ISA bus edge connector. To help you locate the signals more easily, the connector is shown in its physical layout position. The power supply to the board comes from the ISA bus, and includes +5V and ±12V power supplies. Decoupling capacitors are placed on these power supplies to minimize the voltage ripple. The TC signal from the ISA bus is filtered by R58 and C33.

3.3 GLUE LOGIC

See Appendix A, Sheet 4 for a diagram of this circuitry.

With the exception of the seven decoupling capacitors on the V_{DD} net, the components of this module are not required in the motherboard application. This circuit creates the correct environment for PC87351 evaluation on the PC87351EB by providing an interface between the on-chip KBC module and the X-Bus, which is not available on the ISA bus.

Two data switches connect the PC87351 data bus to the system: U10 connects to the ISA bus, and U5 to the X-Bus. Only the KBC module of the PC87351 needs to be connected to the X-Bus. The PAL controls the U10 and U5 switches. See Figure 3-1.

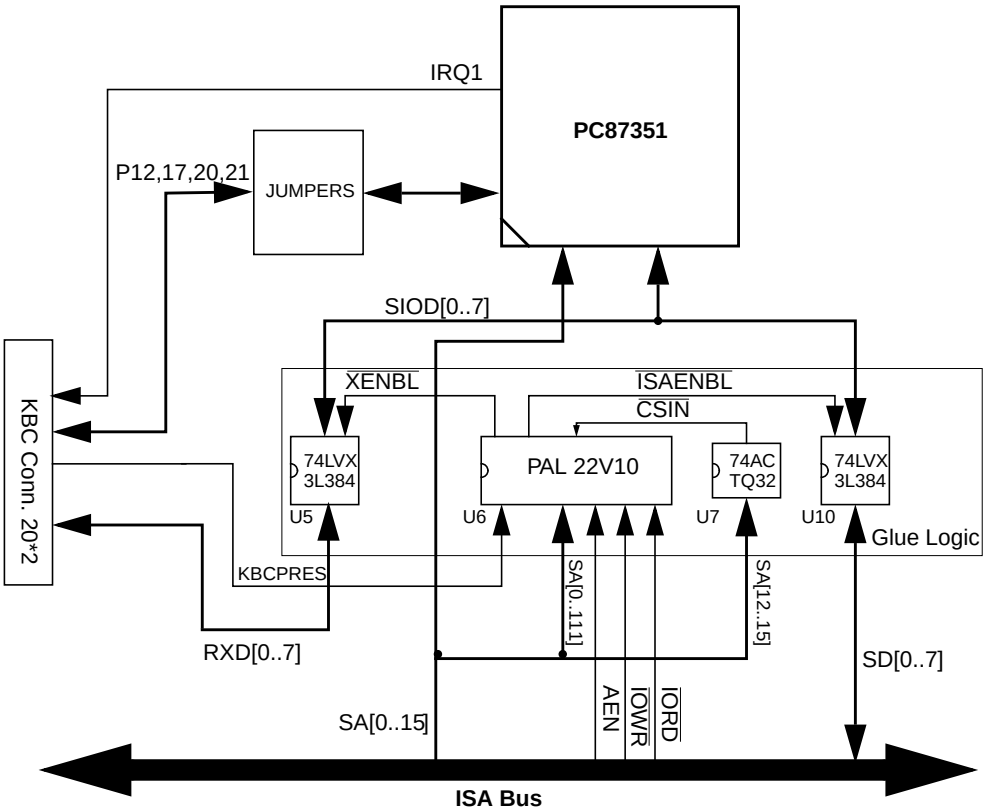


Figure 3-1. ISA Bus and X-Bus Data Architecture

Switch enabling is based on the ISA access address. The switches are controlled by two of the PAL U6 outputs, $\overline{\text{XENBL}}$ and $\overline{\text{ISAENBL}}$.

The ISA switch, U10, is enabled for any read or write access from/to any SuperI/O module located at any address, except the KBC legacy addresses: 60 and 64.

The X-Bus switch, U5, is enabled for any read or write access from/to the KBC module, only when it is enabled in its legacy addresses, as described above.

One 22V10 PAL device, U6, and one 74ACTQ32, U7, are used in this block. The 74ACTQ32 decodes the high ISA address bits A12-A15, and provides the PAL with the $\overline{\text{CSIN}}$ signal that is active low when all the high address bits are zero. The PAL controls the data switches:

- The $\overline{\text{ISAENBL}}$ signal is active on all I/O cycles, except when the address is 60, 64h (KBC legacy address spaces).
- The $\overline{\text{XENBL}}$ signal is active only on I/O cycles with address 60, 64h (KBC legacy address space).

Jumpers on the extension board route P12,17,20,21 signals to the PC87351 chip.

The PAL facilitates automatic hardware configuration for the KBC cable. For further details, see Section 2.5.5 and Figure 2-1.

3.4 DEBUG RESET CIRCUIT

See Appendix A, Sheet 4 for a diagram of this circuit.

This circuit allows you to reset the chip, at any time, by pressing the SW4 switch located near the bracket. It also allows you to disconnect the reset signal from the ISA bus by removing the JP4 jumper. For a description of this jumper, see Section 2.5.2. See also Section 2.6 for software configuration details.

3.5 PC87351 CHIP

See Appendix B, Sheet 2, for a diagram of the PC87351 chip connections.

This block contains the PC87351 chip, U1 on the extension board. U1 interfaces directly with the ISA bus, with the exceptions of the 8-bit data bus that is connected by the U10 switch (Appendix A, Sheet 4) and IRQ1,3 which are connected by JP14 jumper on the extension board (Appendix B, Sheets 2, 3). Other external elements, such as decoupling capacitors, pull-up and pull-down resistors are also required.

3.6 BATTERY CIRCUIT

This circuit includes a 3V lithium battery, CR2335, BT1. It serves to keep the wakeup events configuration valid when the system is powered off.

You do not need any external components to comply with the UL safety standard; all the necessary protection circuitry is on-chip.

The decoupling capacitors, C31 and C11, on the extension board help prevent noise on the V_{BAT} line. XBT2 is an optional socket for a smaller, CR2032 type, battery. The R82 resistor serves only for current measuring.

The V_{BAT} jumper on the extension board enables you to measure the battery current consumption of the PC87351 chip. This jumper should always be inserted.

3.7 FDC

See Appendix A, Sheet 7 for a diagram of the FDC.

You can connect the FDC of the PC87351 to a maximum of two Floppy Disk Drives via a 34-pin standard header, J10. Standard 1 KΩ pull-ups (RN2) are used on all input signals.

3.8 UART1 AND UART2

See Appendix A, Sheet 8 for a diagram of the UARTs.

Each serial port connector, J1 and J2, is a 10-pin dual-row header. The PC87351 chip interfaces these connectors through two DS14185 devices, U1 and U2, respectively. DS14185 is an RS-232 compliant 3-driver/5-receiver chip, manufactured by National Semiconductor. This chip uses the +5V and ±12V power supplies, assuring the most cost-effective implementation and minimum chip count in PC desktop applications. A standard EMI filter circuit is provided for each port (R1-R8/C66-C73 and R9-R16/C74-C81).

Note The pinout matches the IDC10-to-DB9 adapter cable supplied with the package. For further details, see Section 2.3.

The PC87351 chip's wakeup module can sense the state of the $\overline{RI1}$ and $\overline{RI2}$ serial port inputs. This feature supports applications in which an external modem ring signal wakes up the system. To keep these two inputs alive during system power-off, the corresponding line receivers are separated from the DS14185 devices, powered from the standby power supply, and consume very little power. If your application does not implement the above feature, the U3 line receiver can be omitted.

Note The standby voltage V_{SB} on the extension board is referred to as V_{CCH} on the base board.

3.9 INFRARED

See Appendix A, Sheet 9 for a diagram of this module.

A 9-pin D-type female connector, J12, interfaces the PC87351 chip with the supplied analog IRFE module. J12 is located on the bracket for easy access.

The serial resistor R34 (33 Ω) on the IRTX signal from the PC87351 protects the signal from transmission effects.

When the IRFE is not connected to the board, pull-up resistors R35, R38, R39, R37 and R36 (150 KΩ) assure legal logic levels for the IRRX1 input signal. If your application implements the IRFE on the same motherboard so that it is always present, omit these resistors.

The IRFE supports FIR, MIR, SIR and Sharp-IR protocols, as well as TV-remote with demodulation outside the PC87351. See Section 4.3.8 for the header pinout. See also the IRFE documentation for a full description of its features.

3.10 PARALLEL PORT

See Appendix A, Sheet 10, for a diagram of the parallel port.

The IEEE 1284 parallel port on the PC87351 is connected to a standard DB25 connector, J13, on the board's bracket via the ECP terminations.

The PC87351 can route the FDD signals to the parallel port connector. This means that a FDD device can be connected to this DB25 connector. For the setting for this option see the *PC87351 Datasheet.*

3.11 FAN CONTROL CIRCUIT

The PC87351 chip includes a fan control which supports two fans. The PC87351 generates a PWM (Pulse Width Modulation) signal at the fan output according to a predefined frequency and width. External circuitry is needed to convert the 5V PWM output to the 12V logic level used by the fan.

There is one control circuit that can be connected either to Fan0 or to Fan1. The JP5 jumper on the extension board selects which fan is connected to the fan circuit.

JP8 on the extension board routes the fan control to the fan connector J2 on the extension board. It selects either the output from the fan control circuit, or the direct output from the PC87351 chip. This enables the use of a fan that can be connected directly to the PWM signal.

Note When using a fan that connects directly to PWM, it is your responsibility to comply with the PC87351 electrical specifications (see the *PC87351 Datasheet).*

Before using the fan, set JP6 or JP9 according the desired configuration. See Section 2.5.3 for more details. See Figure 3-2 for Fan Control Circuit Layout.

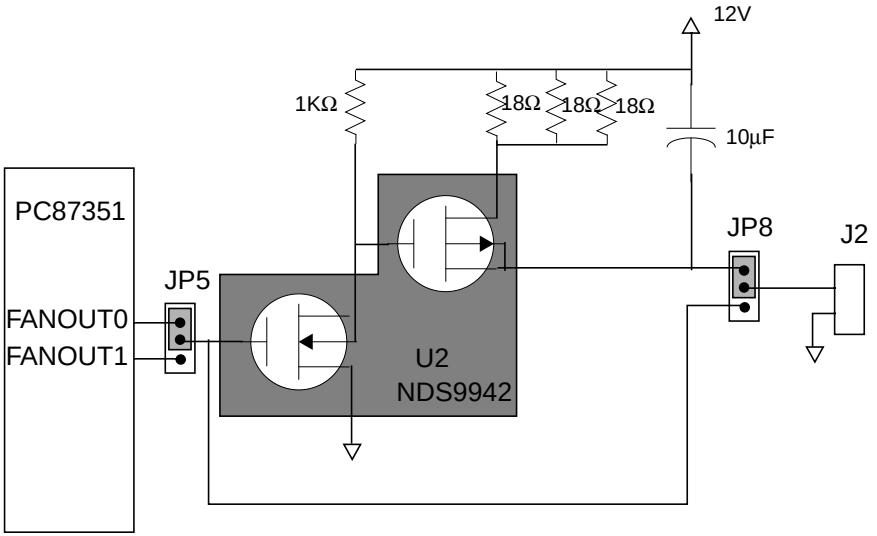


Figure 3-2. Fan Control Circuit

For more details, see Appendix B, Sheet 4.

3.12 ISP

An ISP, U8 on the extension board, is used to enforce a low logic level on the IRQ1 signal during booting, thus enabling a proper setup of the keyboard in SIRQ mode. After booting, you must configure the PC87351 chip to toggle the GPIO16/IRQ12 pin and to work in a parallel IRQ mode. The ISP detects the toggle and releases the IRQ1 signal.

For more information about the configuration of the PC87351 chip see Section 2.6.1.

The ISP device, a Lattice 1032E, is programmed by a PC parallel port connected to a single-row 8-bit header, J10. In a regular mode, it is not necessary to program the ISP since it should be already programmed.

Seven jumpers are reserved for future implementations.

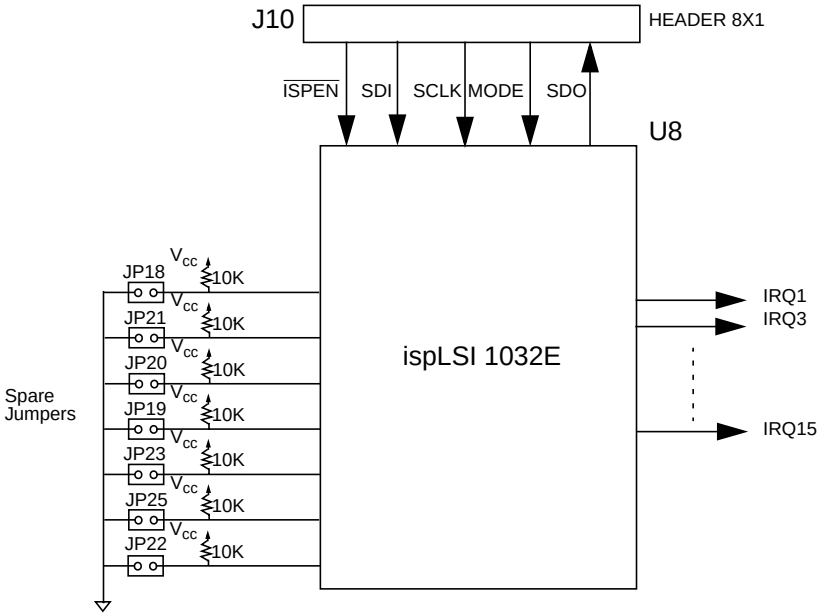


Figure 3-3. ISP Block

For more details, see Appendix B, Sheet 3.

3.13 GPIO PORTS AND PME

See Appendix B, Sheet 4, for a diagram of the GPIO ports and the PME.

3.13.1 GPIO1

The GPIO1 port is connected to a dual-row, 10-pin header, J4 on the extension board. GPIO1 has eight signals: GPIO10-GPIO17. Except for GPIO17, all the signals are duplicated on the PC87351 chip to two sets of pins. To allow evaluation of each of the two sets, two bus changers U5, U3 on the extension board, are used as shown in Figure 3-4.

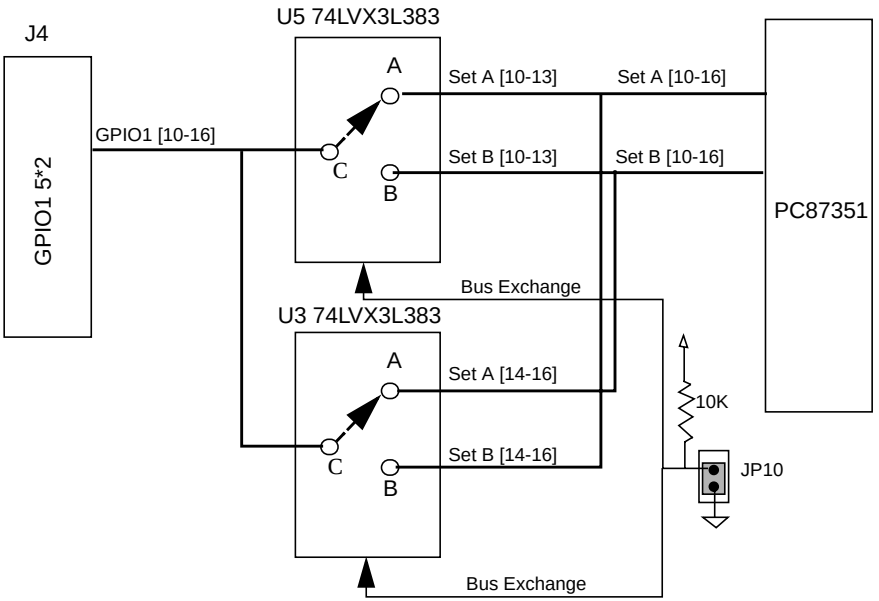


Figure 3-4. GPIO1 Circuit

For more details, see Appendix B, Sheet 4.

3.13.2 GPIO2

The GPIO2 port is accessible on a dual-row, 10-pin header, J3 on the extension board. To use the port, set the jumpers JP12, JP6, JP9 on the extension board according to Section 2.5.3.

3.13.3 PME Connector

A dual-row, 10-pin header, J1 on the extension board connects the multiplexed pins: PME1/$\overline{\text{RING}}$ and PME2/$\overline{\text{SUSP}}$ of the PC87351 chip.

Bits 0,2 of SIOCF4 register of the PC87351 chip, determine the functionality of the pins as described in the two tables below:

Table 3-1. PME1/$\overline{\text{RING}}$ Pin

SIOCF4, Bit 0	Function of PME1/$\overline{\text{RING}}$ Pin
0	RING
1	PME1

Table 3-2. PME2/$\overline{\text{SUSP}}$ Pin

SIOCF4, Bit 2	Function of PME2/$\overline{\text{SUSP}}$ Pin
0	SUSP
1	PME2

The PME1, PME2 and $\overline{\text{RING}}$ signals are used as wake up events.

For more details see the *PC87351 Datasheet.*

3.14 PS/2 KEYBOARD AND MOUSE CONNECTORS

See Appendix A, Sheet 12 for a diagram of these connectors.

The PC87351 directly interfaces with a keyboard and a PS/2 type mouse. The KBCLK and KBDAT, MCLK and MDAT signals are connected to the keyboard and mouse connectors, J7 and J6 (MINI-DIN 6-pin type). They are located at the top of the board for easy access. A standard EMI filter circuit is provided (L1-6, C47-52). In a high-end system, you may also implement a protection circuit on the power pins of J7 and J6. See Sections 4.3.4 and 4.3.5 for connector pinout.

3.15 KBC CONNECTOR

See Appendix A, Sheet 13, for a diagram of this connector.

Only motherboards with a discrete KBC chip in the DIP socket can be used to evaluate the KBC module from the PC87351 on the PC87351EB.

You can connect the PC87351 KBC block to the motherboard via a 40-pin header, J4. (See Section 4.3.3 for J4 pinout). Connect J4, located on the left side of the board, with the supplied cable to the KBC socket on the motherboard. (See Section 2.5.4 for system installation procedures). Bear in mind that you may have to replace the 8042 KBC chip, which must be a 40-pin DIP component, with a 40-pin socket.

The KBC module uses two IRQ signals. IRQ1 is connected by the J4 connector, pin 12. IRQ12, used by the PS/2 mouse, is connected directly to the ISA connector.

Some of the GPIO lines on the original 8042 device are not available on the PC87351. Instead, pull-up resistors RN1 (1 KΩ, 9-resistor pack) are connected to these pins to prevent them from floating. Pins P20 and P21 are pulled-up by resistors R78 and R77 (10 KΩ). These two signals are open drain, and are used as the GATEA20 and the RESET signals from the KBC.

3.16 TEST CONNECTORS

See Appendix B, Sheet 2 for a diagram of the test connectors.

Connectors XJ4 (A, B, C and D) are used to mount the extension board. All the PC87351 pins are accessible for testing on XJ4 connector pins. The XJ4E connector carries the 12V voltage for the Fan circuit from the base board to the extension board.

Chapter 4
SPECIFICATIONS

4.1 INTRODUCTION

The PC87351EB is designed to be mounted in a PC-AT slot.

4.2 PHYSICAL SPECIFICATIONS

The four-layer PC87351EB measures 231 mm x 107.8 mm. It is designed to be used in a laboratory environment within normal commercial temperature and humidity ranges:

Temperature : 0 °C to + 50 °C
Humidity : 0% to 90%, no condensation

4.3 BASE BOARD CONNECTORS

The PC87351 base board has 11 connectors, described in this section. Table 4-1 shows the function and type of each connector.

Table 4-1. PC87351EB Connector List

Connector	Description
J1	SERIAL1 Connector, double-row 10-pin header
J2	SERIAL2 Connector, double-row 10-pin header
J4	KBC Connector, double-row 40-pin header
J6	PS/2 Mouse, MINI-DIN 6-pin round connector
J7	PS/2 Keyboard, MINI-DIN 6-pin round connector
J8	Standby Power Connector, single-row 3-pin header
J10	FDC Connector, double-row 34-pin header
J12	IR Connector, DB9 female connector
J13	Parallel Port Connector, DB25 female connector
P1	ISA Bus Connector, XT, edge 62-pin
P2	ISA Bus Connector, AT, edge 36-pin

4.3.1 SERIAL1 Connector, J1

A double-row, 10-pin header.

Table 4-2. SERIAL1 Connector, J1

Signal	Pin No.	Pin No.	Signal
DCD1F	1	2	DSR1F
$\overline{\text{SIN1F}}$	3	4	RTS1F
$\overline{\text{SOUT1F}}$	5	6	CTS1F
DTR1F	7	8	RI1F
GND	9	10	N.C.

4.3.2 SERIAL2 Connector, J2

A double-row, 10-pin header.

Table 4-3. SERIAL2 Connector, J2

Signal	Pin No.	Pin No.	Signal
DCD2F	1	2	DSR2F
$\overline{\text{SIN2F}}$	3	4	RTS2F
$\overline{\text{SOUT2F}}$	5	6	CTS2F
DTR2F	7	8	RI2F
GND	9	10	N.C.

4.3.3 KBC Connector, J4

A double-row, 40-pin header whose pinout is similar to the DIP 40-pin KBC socket on a PC motherboard. Only some of the signals are supplied by the PC87351. The rest are not connected, or are connected to 1 KΩ pull-up resistors.

Table 4-4. KBC Connector, J4

Signal	Pin No.	Pin No.	Signal
N.C.	1	2	KBCV
N.C.	3	4	N.C.
N.C.	5	6	P27

Table 4-4. KBC Connector, J4 (Continued)

Signal	Pin No.	Pin No.	Signal
N.C.	7	8	P26
N.C.	9	10	N.C.
N.C.	11	12	IRQ1
N.C.	13	14	P17
N.C.	15	16	P16
N.C.	17	18	P15
N.C.	19	20	P14
N.C.	21	22	P13
RXD0	23	24	P12
RXD2	25	26	P11
RXD3	27	28	P10
RXD4	29	30	N.C.
RXD5	31	32	N.C.
RXD6	33	34	P23
RXD7	35	36	P22
RXD2	37	38	P21
GND	39	40	P20

4.3.4 Mouse Connector, J6

A MINI-DIN 6-pin round connector.

Table 4-5. Mouse Connector, J6

Pin No.	Signal
1	MDATC
2	N.C.
3	GND
4	MOUVCC
5	MCLKC
6	N.C.

4.3.5 KBD Connector, J7

A MINI-DIN 6-pin round connector.

Table 4-6. KBD Connector, J7

Pin No.	Signal
1	KBDATC
2	N.C.
3	GND
4	KBDVCC
5	KBCLKC
6	N.C.

4.3.6 Standby Power Connector, J8

A 3-pin header.

Table 4-7. Standby Power Connector, J8

Pin No.	Signal
1	N.C.
2	VHEXT
3	GND

4.3.7 FDC Connector, J10

A double-row, 34-pin header. J10 can connect up to two Floppy Disk Drives.

Table 4-8. FDC Connector, J10

Signal	Pin No.	Pin No.	Signal
GND	1	2	DENSEL
GND	3	4	N.C.
GND	5	6	DRATE0
GND	7	8	$\overline{\text{INDEX}}$
N.C.	9	10	$\overline{\text{MTR0}}$

Table 4-8. FDC Connector, J10 (Continued)

Signal	Pin No.	Pin No.	Signal
GND	11	12	$\overline{DR1}$
GND	13	14	$\overline{DR0}$
GND	15	16	$\overline{MTR1}$
MSEN1	17	18	$\overline{DIR}$
GND	19	20	$\overline{STEP}$
GND	21	22	$\overline{WDATA}$
GND	23	24	$\overline{WGATE}$
GND	25	26	$\overline{TRK0}$
MSEN0	27	28	$\overline{WP}$
N.C.	29	30	$\overline{RDATA}$
GND	31	32	$\overline{HDSEL}$
N.C.	33	34	$\overline{DSKCHG}$

4.3.8 IRFE Connector, J12

A 9-pin D-Type, female, right-angle bracket mounted connector, with two additional pins for shield connection

.

Table 4-9. IRFE Connector, J12

Pin No.	TX/RX Signals	Control Signals	PnP Identification Signals	Power
1	IRTXC			
2				GND
3			ID3 (Not Used)	
4	IRRX2	IRSL0	ID0 (Not Used)	
5		IRSL1	ID1 (Not Used)	
6	IRRX1			
7				IRVCC
8		IRSL2	ID2 (Not Used)	
9	N.C.			
10, 11				SHIELD

4.3.9 Parallel Port Connector, J13

A DB25 female connector.

Table 4-10. Parallel Port Connector, J13

Pin No.	Signal
1	$\overline{\text{RSTB}}$
2 - 9	RPD0-RPD7
10	$\overline{\text{RACK}}$
11	RBUSY
12	PE
13	SLCT
14	AFD
15	$\overline{\text{ERR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{RSLIN}}$
18 - 25	GND

4.3.10 ISA XT and AT Connectors, P1 and P2

The pinout for these connectors meets ISA specifications.

4.4 EXTENSION BOARD CONNECTORS

4.4.1 PME Connector, J1

A 10-pin, dual-row header.

.

Table 4-11. PME Connector, J1

Pin No.	Signal
1	PME1/$\overline{\text{RING}}$
2	PME2/$\overline{\text{SUSP}}$
3-8	N.C.
9,10	GND

4.4.2 Fan Connector, J2

A 2-pin, dual-row header.

Table 4-12. Fan Connector, J2

Pin No.	Signal
1	GND
2	FANOUT

4.4.3 GPIO2 Connector, J3

A 10-pin, dual-row header.

Table 4-13. GPIO2 Connector, J3

Pin No.	Signal
1	GPIO20
2	GPIO21
3	GPIO22
4-8	N.C.
9,10	GND

4.4.4 GPIO1 Connector, J4

A 10-pin, dual-row header.

Table 4-14. GPIO1 Connector, J4

Pin No.	Signal
1	GPIO10
2	GPIO11
3	GPIO12
4	GPIO13
5	GPIO14
6	GPIO15
7	GPIO16
8	GPIO17
9,10	GND

4.4.5 ISP Connector, J10

An 8-pin, single-row header.

Table 4-15. ISP Connector, J10

Pin No.	Signal
1	V_{DD}
2	ISPEN
3	SDI
4	SCLK
5	MODE
6	SDO
7,8	GND

4.5 CURRENT REQUIREMENTS

The PC87351EB board requires +5V and ±12V.

Table 4-16 shows the maximum calculated power consumption for each chip.

Table 4-16. Max Power Consumption

Chip	Quantity	+5V Current [mA]	+12V Current [mA]	−12V Current [mA]
PC87351	1	32[a]		
DS14185	2	60	44	-56
DS14C89	1	1		
PAL22V10	1	140		
74ACTQ32	1	6		
74F132	1	18		
74LVX3L384	4	80		
74LVX3L383	2	40		
ispLSI1032E	1	190		
Total		567	44	-56

a. Typical value

The maximum calculated power consumption for the board is:

567 mA @ +5V
44 mA @ +12V
−56 mA @ −12V

Appendix A
BASE BOARD SCHEMATIC DIAGRAMS

The following pages contain the schematics diagrams for the PC87351EB base board.

REVISIONS

ECN#	PCB 551521	ASS 980521	SCH	DESCRIPTION	DATE	APPROVED
			1.0	INITIAL VERSION	07 JAN 1997	IACOB T.
			1.1	DDR REVIEW	20 JAN 1997	IACOB T.
			1.2	UPDATE FOR PC87309 SUPPORT	03 FEB 1997	IACOB T.
	682-001/A	682-001/A	1.3	RELEASED VER AFTER BACKANOTATION	09 FEB 1997	IACOB T.
184	682-001/A	686-001/A	1.4	CONFIGURATION RESISTORS, U2, U1 UPDATE FOR PC87309EB USE ONLY. ASSEMBLY BASE NUMBER --> 686	04 MAR 1997	IACOB T.
186	682-002/A	682-002/A	2.0	NEW PCB LAYOUT INCLUDING: PULL-DOWN OPTION ON STRAP PINS, SOCKET OPTION FOR U4.	23 MAR 1997	IACOB T.
189	682-002/A	682-002/B 682-002/C	2.1	R41 680R PULL-DOWN R41 10K PULL-DOWN, U8 CMOS	09 APR 1997	IACOB T.

DESIGN FILES (ORCAD 386+)

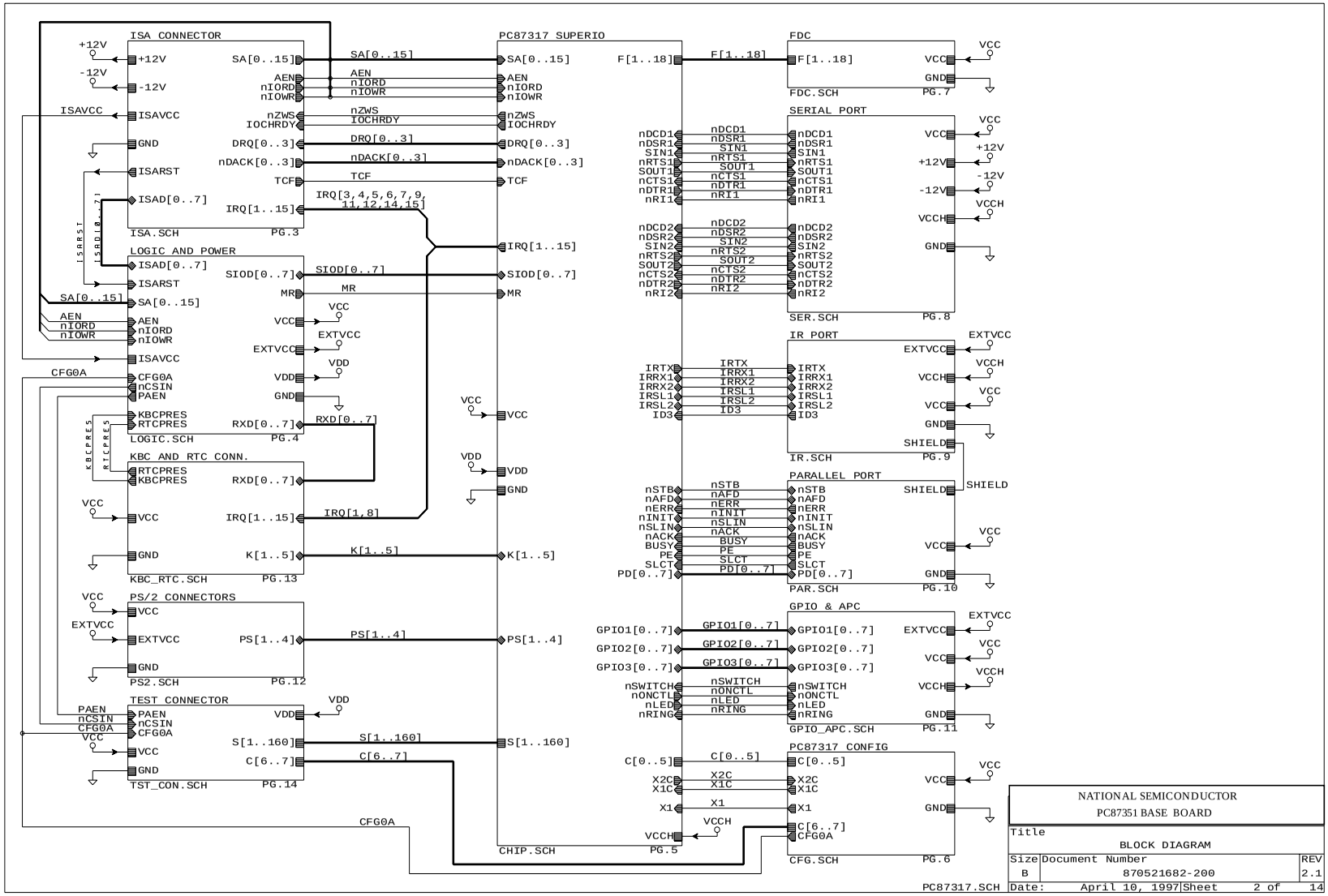
SCHEMATIC:	COVER.SCH	PG.1	COVER PAGE
	PC87317.SCH	PG.2	BLOCK DIAGRAM
	ISA.SCH	PG.3	ISA CONNECTOR
	LOGIC.SCH	PG.4	GLUE LOGIC
	CHIP.SCH	PG.5	PC87317 CHIP CONNECTIONS
	CFG.SCH	PG.6	PC87317 CONFIGURATION & CLOCK SOURCES
	FDC.SCH	PG.7	FLOPPY DISK DRIVE CONNECTOR
	SER.SCH	PG.8	SERIAL PORTS DRIVERS & CONNECTORS
	IR.SCH	PG.9	INFRARED PORT CONNECTOR
	PAR.SCH	PG.10	PARALLEL PORT TERMINATIONS & CONNECTOR
	GPIO_APC.SCH	PG.11	GPIO AND ADVANCED POWER CONTROL
	PS2.SCH	PG.12	PS/2 KEYBOARD AND PS/2 MOUSE
	KBC_RTC.SCH	PG.13	KBC AND RTC CABLE CONNECTORS
	TST_CON.SCH	PG.14	TEST CONNECTORS
LIBRARY:	317EB.LIB		NATIONAL SEMICONDUCTOR LIBRARY

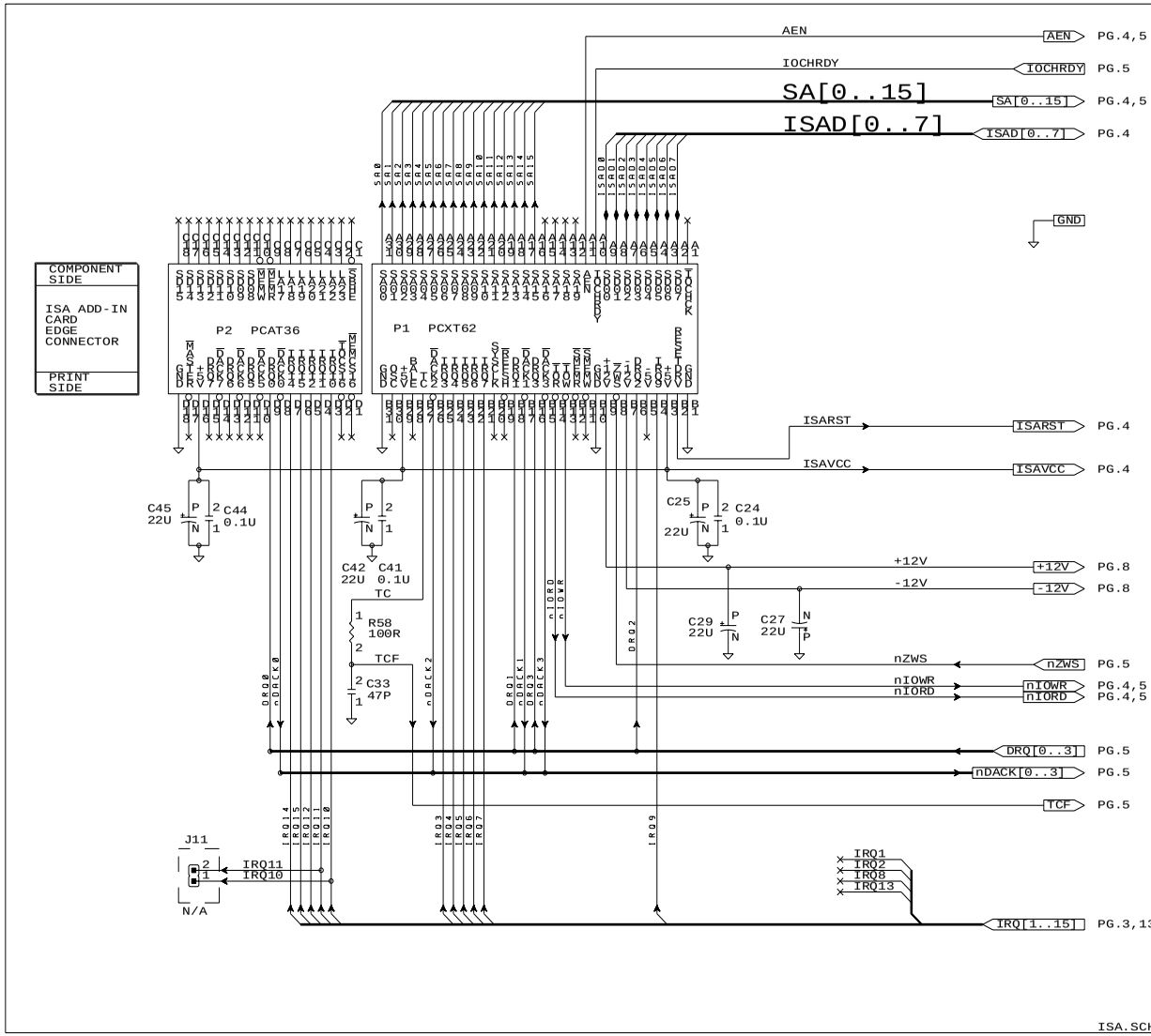
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
ASSEMBLED PCB P/N 980521694-001

Title: COVER PAGE

Size	Document Number	REV
B	870521682-200	2.1

COVER.SCH Date: April 10, 1997 Sheet 1 of 14

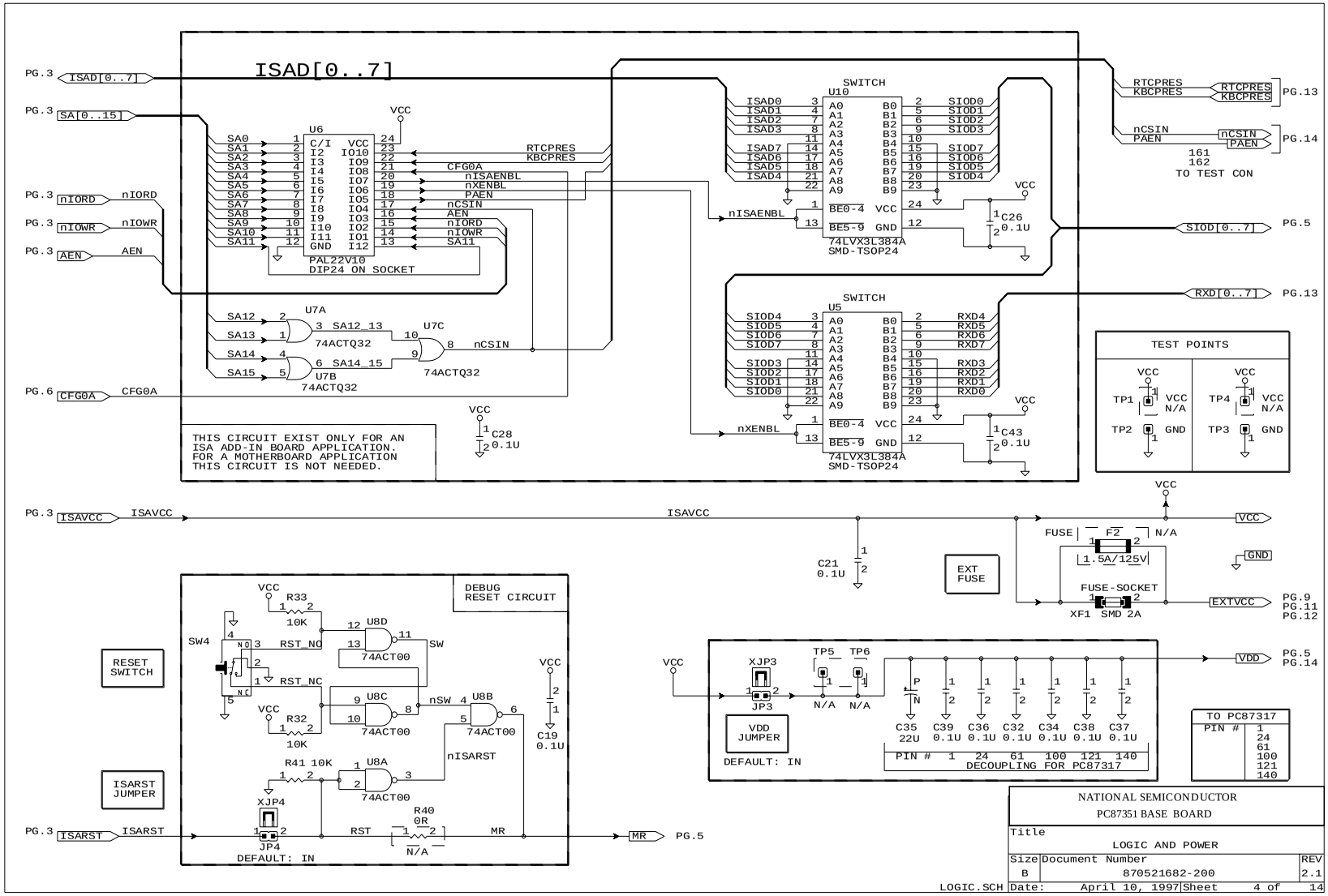

ISA CONNECTOR
+12V
-12V
ISAVCC
GND
ISARST
ISAD[0..7]
SA[0..15]
AEN
nIORD
nIOWR
nZWS
IOCHRDY
DRQ[0..3]
nDACK[0..3]
TCF
IRQ[1..15]
ISA.SCH
PG.3
LOGIC AND POWER
SIOD[0..7]
MR
VCC
EXTVCC
VDD
CFG0A
nCSIN
PAEN
KBCPRES
RTCPRES
RXD[0..7]
LOGIC.SCH
PG.4
KBC AND RTC CONN.
IRQ[1..15]
K[1..5]
KBC_RTC.SCH
PG.13
PS/2 CONNECTORS
PS[1..4]
PS2.SCH
PG.12
TEST CONNECTOR
S[1..160]
C[6..7]
TST_CON.SCH
PG.14
PC87317 SUPERIO
IRQ[3,4,5,6,7,9,
11,12,14,15]
IRQ[1,8]
CHIP.SCH
PG.5
F[1..18]
FDC
FDC.SCH
PG.7
SERIAL PORT
nDCD1
nDSR1
SIN1
nRTS1
SOUT1
nCTS1
nDTR1
nRI1
nDCD2
nDSR2
SIN2
nRTS2
SOUT2
nCTS2
nDTR2
nRI2
SER.SCH
PG.8
IR PORT
IRTX
IRRX1
IRRX2
IRSL1
IRSL2
ID3
SHIELD
IR.SCH
PG.9
PARALLEL PORT
nSTB
nAFD
nERR
nINIT
nSLIN
nACK
BUSY
PE
SLCT
PD[0..7]
PAR.SCH
PG.10
GPIO & APC
GPIO1[0..7]
GPIO2[0..7]
GPIO3[0..7]
nSWITCH
nONCTL
nLED
nRING
GPIO_APC.SCH
PG.11
PC87317 CONFIG
C[0..5]
X2C
X1C
X1
CFG.SCH
PG.6
PC87317.SCH
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
Title
BLOCK DIAGRAM
Size
B
Document Number
870521682-200
REV
2.1
Date: April 10, 1997
Sheet 2 of 14

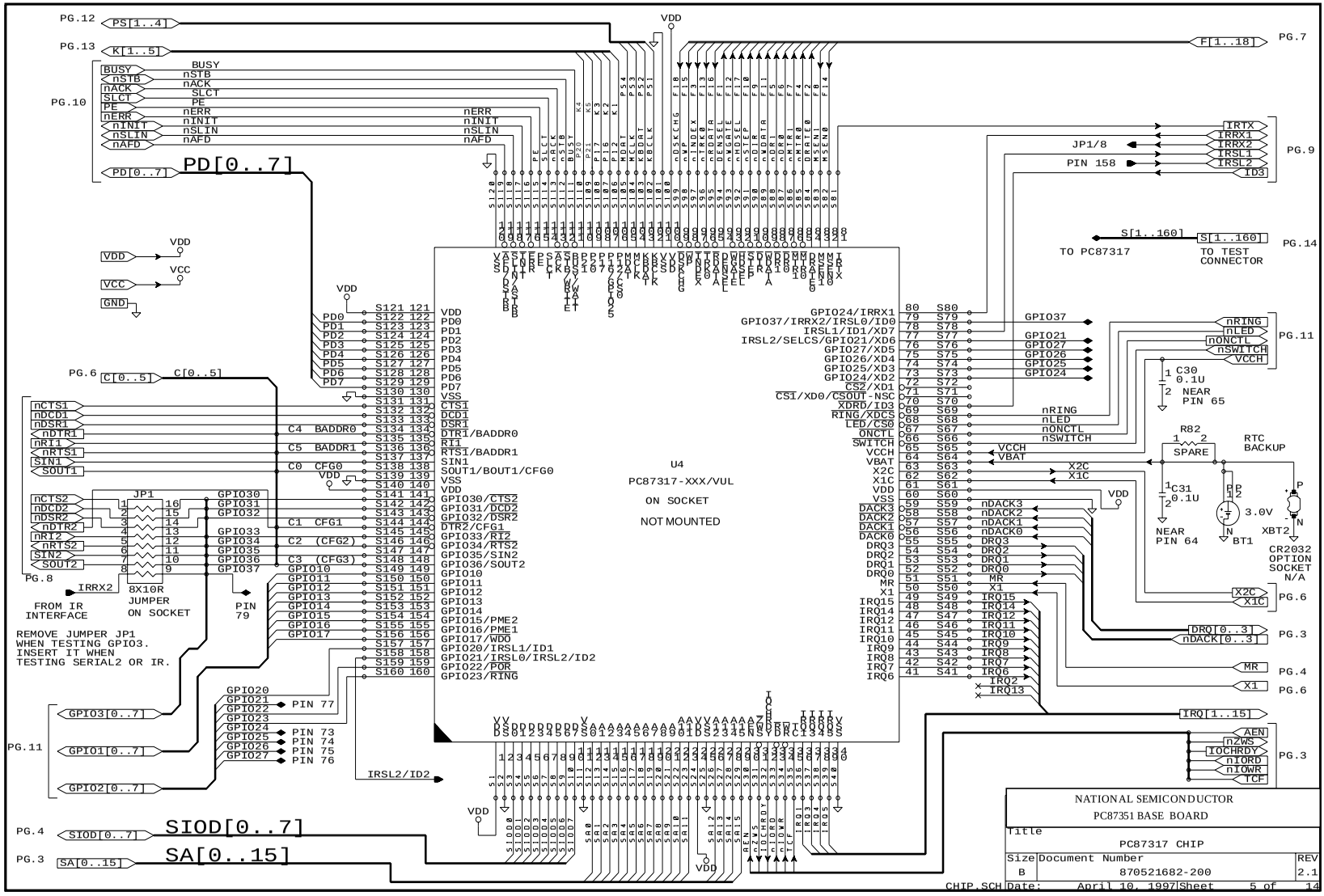


NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD

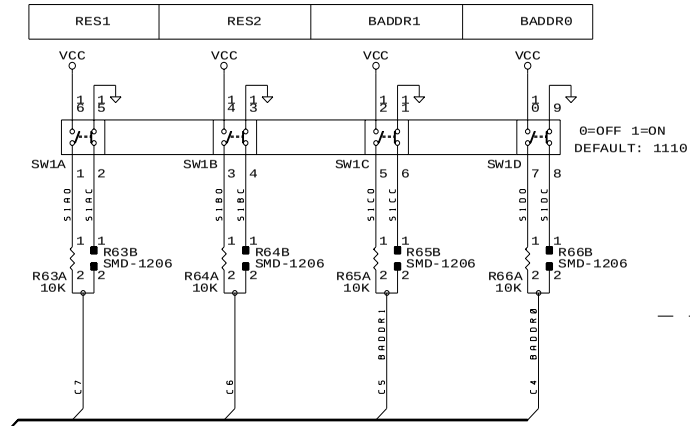
Title		
	ISA CONNECTOR	
Size	Document Number	REV
B	870521682-200	2.1
Date: April 10, 1997	Sheet 3 of 14	

ISA.SCH


ISAD[0..7]
PG.3 ISAD[0..7]
PG.3 SA[0..15]
PG.3 nIORD nIORD
PG.3 nIOWR nIOWR
PG.3 AEN AEN
PG.6 CFG0A CFG0A
U6
PAL22V10
DIP24 ON SOCKET
VCC
RTCPRES
KBCPRES
CFG0A
nISAENBL
nXENBL
PAEN
nCSIN
AEN
nIORD
nIOWR
SA11
U7A
74ACTQ32
SA12_13
U7C
74ACTQ32
nCSIN
U7B
74ACTQ32
SA12_15
C28
0.1U
THIS CIRCUIT EXIST ONLY FOR AN
ISA ADD-IN BOARD APPLICATION.
FOR A MOTHERBOARD APPLICATION
THIS CIRCUIT IS NOT NEEDED.
SWITCH
U10
74LVX3L384A
SMD-TSOP24
C26
0.1U
SIOD[0..7] PG.5
RTCPRES
KBCPRES
PG.13
nCSIN
PAEN
PG.14
161
162
TO TEST CON
RXD[0..7] PG.13
U5
C43
0.1U
TEST POINTS
TP1 VCC N/A
TP2 GND
TP4 VCC N/A
TP3 GND
PG.3 ISAVCC ISAVCC
C21
0.1U
EXT
FUSE
FUSE F2 N/A
1.5A/125V
FUSE-SOCKET
XF1 SMD 2A
EXTVCC
PG.9
PG.11
PG.12
GND
RESET
SWITCH
DEBUG
RESET CIRCUIT
R33
10K
U8D
74ACT00
SW4
RST_NC
SW
U8C
nSW
U8B
R32
10K
C19
0.1U
R41 10K
U8A
nISARST
ISARST
JUMPER
XJP4
JP4
DEFAULT: IN
RST
R40
0R
N/A
MR
PG.5
XJP3
JP3
TP5
TP6
VDD
PG.5
PG.14
VDD
JUMPER
DEFAULT: IN
C35 22U
C39 0.1U
C36 0.1U
C32 0.1U
C34 0.1U
C38 0.1U
C37 0.1U
PIN # 1 24 61 100 121 140
DECOUPLING FOR PC87317
TO PC87317
PIN # 1 24 61 100 121 140
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
Title
LOGIC AND POWER
Size B
Document Number 870521682-200
REV 2.1
LOGIC.SCH
Date: April 10, 1997
Sheet 4 of 14


PD[0..7]
SIOD[0..7]
SA[0..15]
U4
PC87317-XXX/VUL
ON SOCKET
NOT MOUNTED
JP1
8X10R
JUMPER
ON SOCKET
REMOVE JUMPER JP1
WHEN TESTING GPIO3.
INSERT IT WHEN
TESTING SERIAL2 OR IR.
FROM IR
INTERFACE
TO PC87317
TO TEST
CONNECTOR
RTC
BACKUP
CR2032
OPTION
SOCKET
N/A
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
Title
PC87317 CHIP
Size
B
Document Number
870521682-200
REV
2.1
CHIP.SCH
Date:
April 10, 1997
Sheet
5 of
14

NOTE 1: U7D, SW1 AND SW2 ARE NEEDED ONLY FOR THE EVALUATION BOARD. THE REAL APPLICATION NEEDS ONLY SOME PULL-UP RESISTORS.



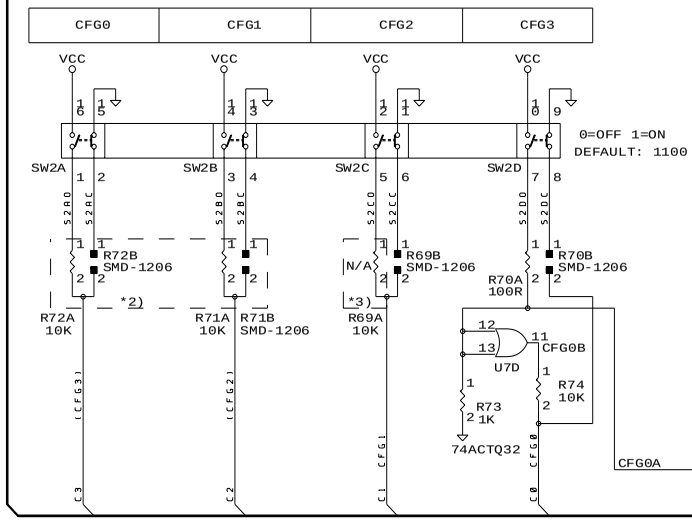


TABLE 1.

BASE ADDRESS		SW1	
		BADDR1	BADDR0
FULL PnP ISA		0	X
PnP MBD	002E	1	1
	015C	1	0
DEFAULT :		1	0

TABLE 2.

CLOCK CONFIG PC87308/307 *1)	SW2	
	CFG3	CFG2
24MHz ON X1	0	0
RESERVED	0	1
48MHz ON X1	1	0
32.768KHz	1	1
DEFAULT :	1	1

TABLE 3.

RESET CONFIG	ENA-BLED	SW2	
		CFG1	CFG0
KBC RTC FDC	Y	X	1
	N	X	0
X-DATA BUFFER	Y	1	X
	N	0 *3	X
PC87317 ONLY	48MHz ON X1		1
CLOCK SOURCE	32.768KHz		0
DEFAULT :		0	0

TABLE 4.

POWER-ON CONFIGURATION SIGNALS						
	BADDR		CFG			
CHIP\SIGNAL	1	0	3	2	1	0
PC87307	√	√	√	√	√	√
PC87308	√	√	√	√	√	√
PC87317	√	√			√	√
PC87309	√	√				√

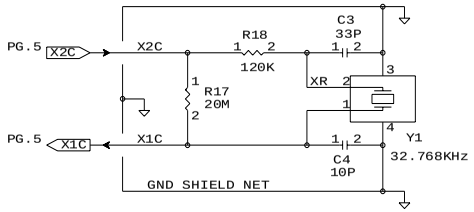
CFG0A — CFG0A — PG.4 PG.14

C[0..5] — PG.5

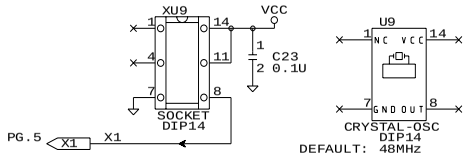
C[6..7] — PG.14

NOTE 2: R72A/B AND R71A/B ARE PROVIDED FOR PC87308/307 SUPPORT ONLY; SEE TABLE 4.

NOTE 3: R69A IS NOT ASSEMBLED SINCE THE X-BUS DATA BUFFER IS NOT IMPLEMENTED IN THIS EVALUATION BOARD.

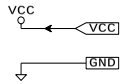


RTC OSCILLATOR & CLOCK MULTIPLIER SOURCE

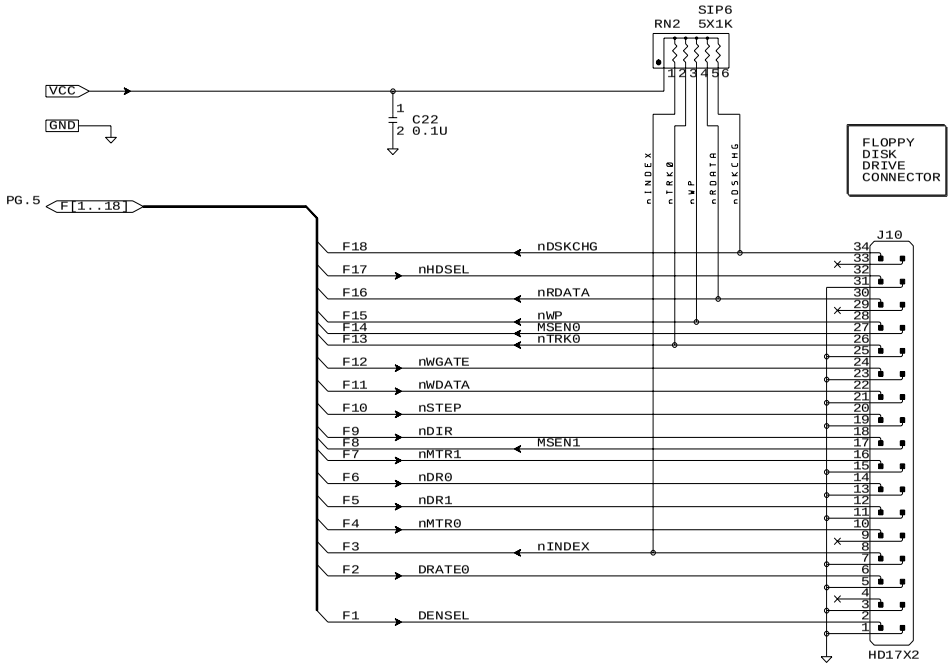


EXTERNAL CLOCK OSCILLATOR

NOTE 5: THE EXTERNAL OSCILLATOR IS NEEDED ONLY IF NOT USING THE ON-CHIP CLOCK MULTIPLIER.

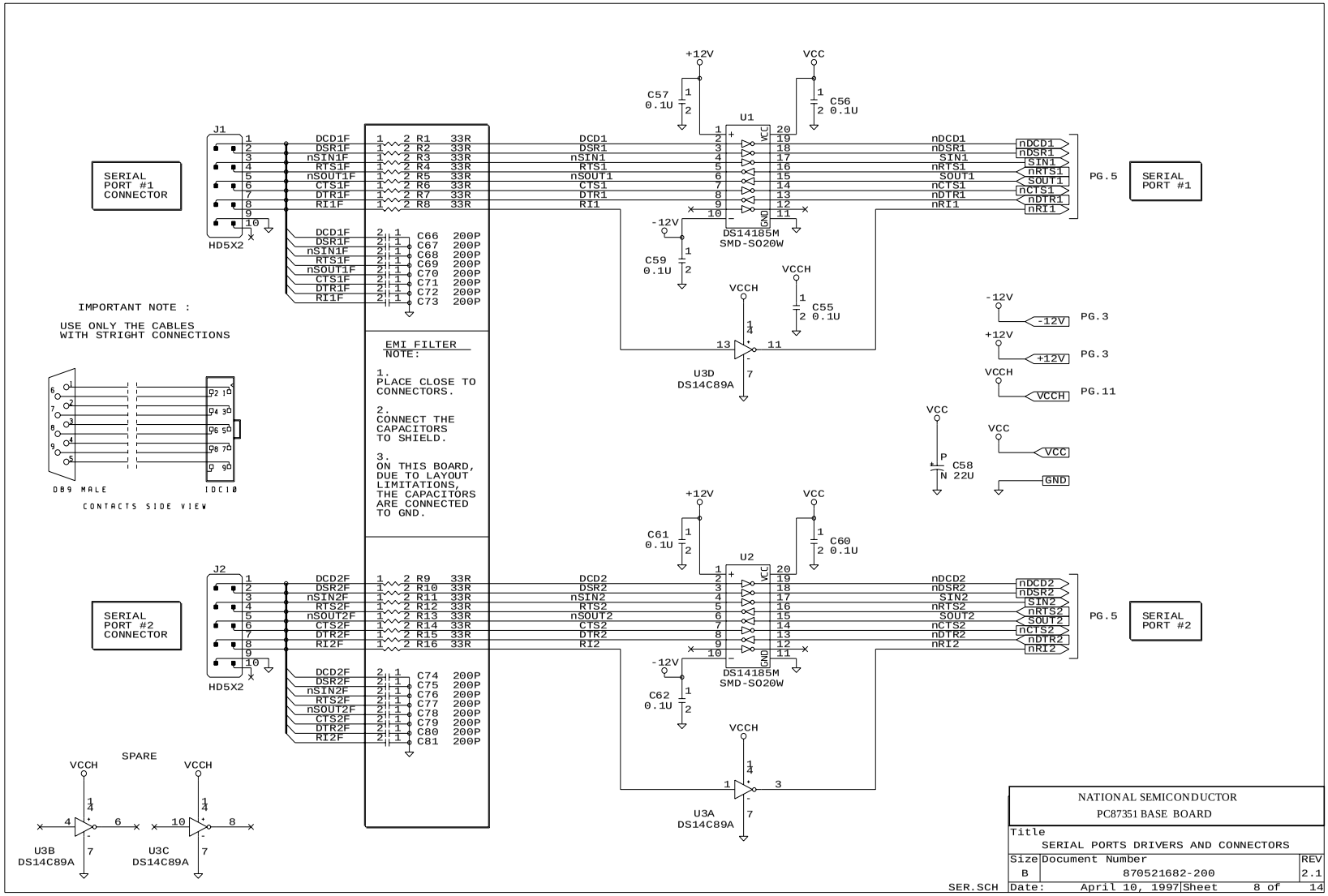


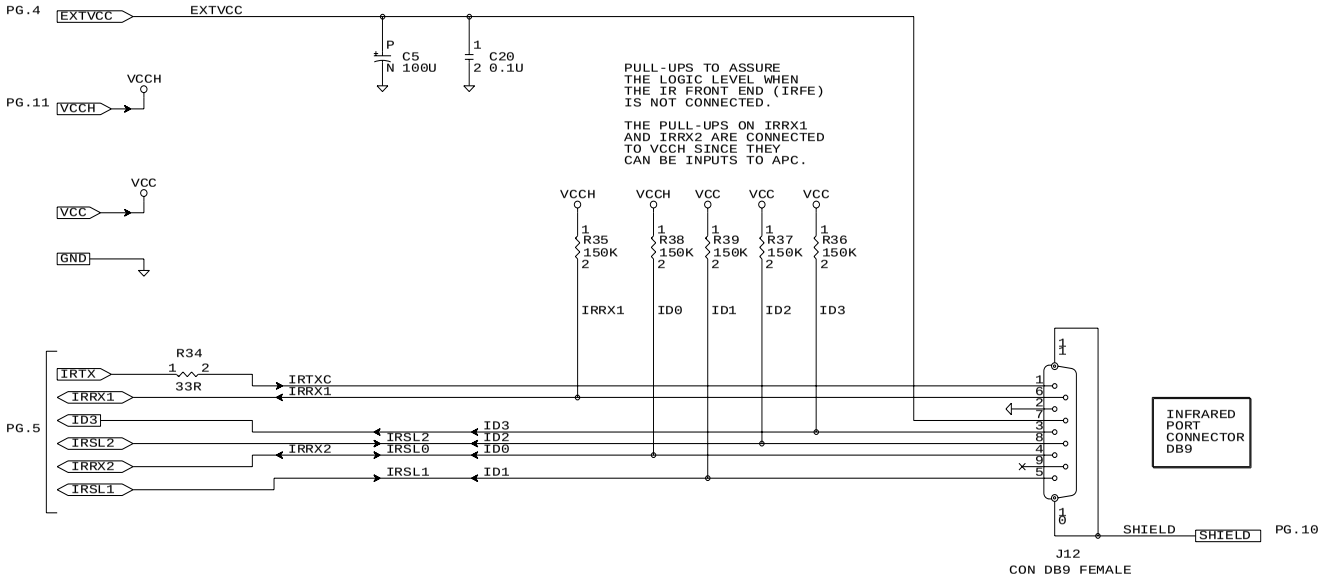
NATIONAL SEMICONDUCTOR PC87351 BASE BOARD	
Title PC87317 CONFIGURATION & CLOCK SOURCE	
Size B	Document Number 870521682-200 REV 2.1
CFG.SCH	Date: April 10, 1997 Sheet 6 of 14



NATIONAL SEMICONDUCTOR PC87351 BASE BOARD		
Title FLOPPY DISK DRIVE CONNECTOR		
Size B	Document Number 870521682-200	REV 2.1
Date: April 10, 1997	Sheet 7 of 14	

FDC.SCH

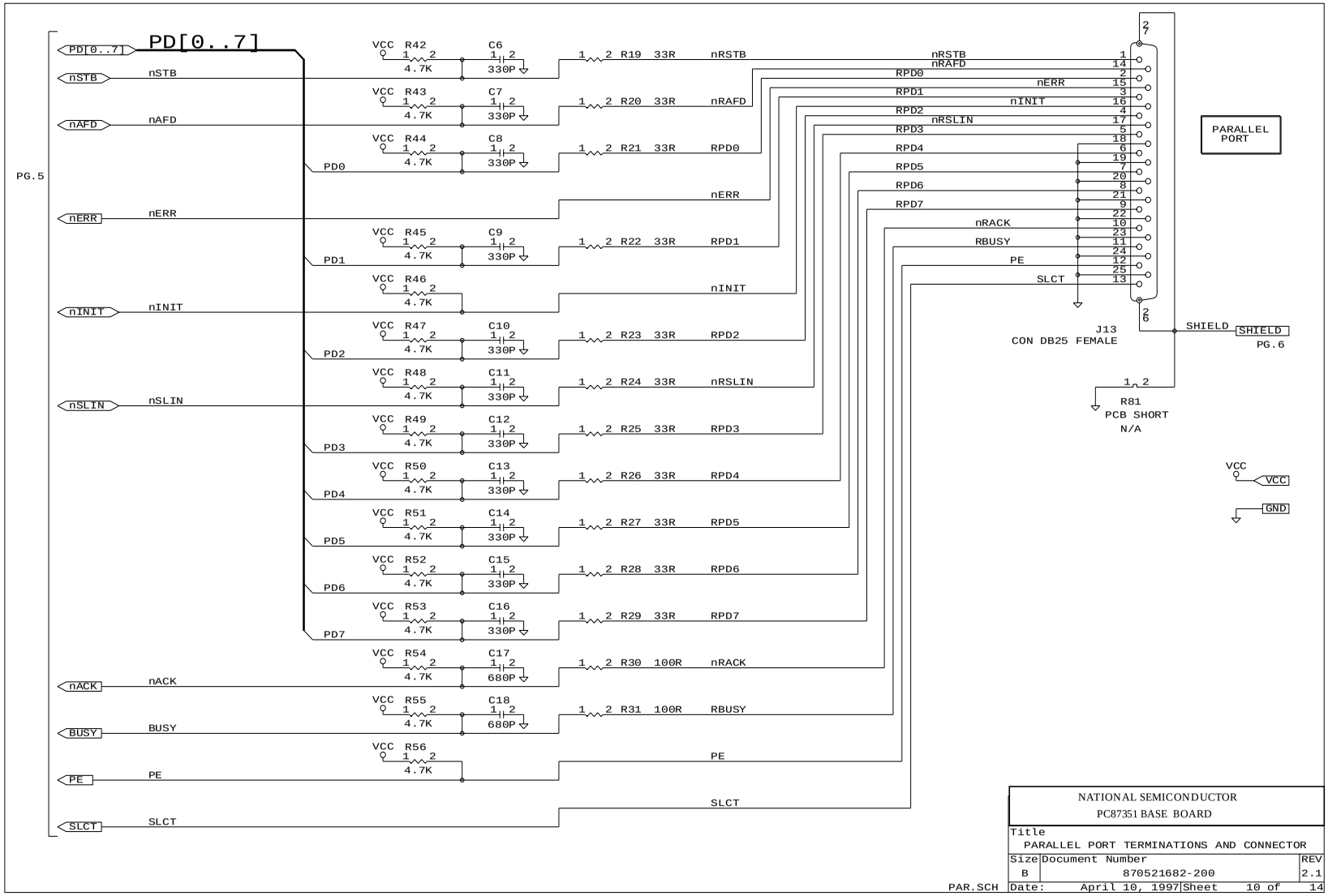

SERIAL PORT #1 CONNECTOR
J1
HD5X2
DCD1F
DSR1F
nSIN1F
RTS1F
nSOUT1F
CTS1F
DTR1F
RI1F
R1 33R
R2 33R
R3 33R
R4 33R
R5 33R
R6 33R
R7 33R
R8 33R
C66 200P
C67 200P
C68 200P
C69 200P
C70 200P
C71 200P
C72 200P
C73 200P
EMI FILTER NOTE:
1. PLACE CLOSE TO CONNECTORS.
2. CONNECT THE CAPACITORS TO SHIELD.
3. ON THIS BOARD, DUE TO LAYOUT LIMITATIONS, THE CAPACITORS ARE CONNECTED TO GND.
IMPORTANT NOTE :
USE ONLY THE CABLES WITH STRIGHT CONNECTIONS
DB9 MALE
IDC10
CONTACTS SIDE VIEW
+12V
VCC
C57 0.1U
C56 0.1U
U1
DS14185M
SMD-SO20W
-12V
C59 0.1U
VCCH
C55 0.1U
U3D
DS14C89A
DCD1
DSR1
nSIN1
RTS1
nSOUT1
CTS1
DTR1
RI1
nDCD1
nDSR1
SIN1
nRTS1
SOUT1
nCTS1
nDTR1
nRI1
PG.5
SERIAL PORT #1
PG.3
PG.11
C58 22U
GND
SERIAL PORT #2 CONNECTOR
J2
DCD2F
DSR2F
nSIN2F
RTS2F
nSOUT2F
CTS2F
DTR2F
RI2F
R9 33R
R10 33R
R11 33R
R12 33R
R13 33R
R14 33R
R15 33R
R16 33R
C74 200P
C75 200P
C76 200P
C77 200P
C78 200P
C79 200P
C80 200P
C81 200P
C61 0.1U
C60 0.1U
U2
C62 0.1U
U3A
DS14C89A
DCD2
DSR2
nSIN2
RTS2
nSOUT2
CTS2
DTR2
RI2
nDCD2
nDSR2
SIN2
nRTS2
SOUT2
nCTS2
nDTR2
nRI2
SERIAL PORT #2
SPARE
U3B
DS14C89A
U3C
DS14C89A
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
Title
SERIAL PORTS DRIVERS AND CONNECTORS
Size B
Document Number 870521682-200
REV 2.1
SER.SCH
Date: April 10, 1997
Sheet 8 of 14

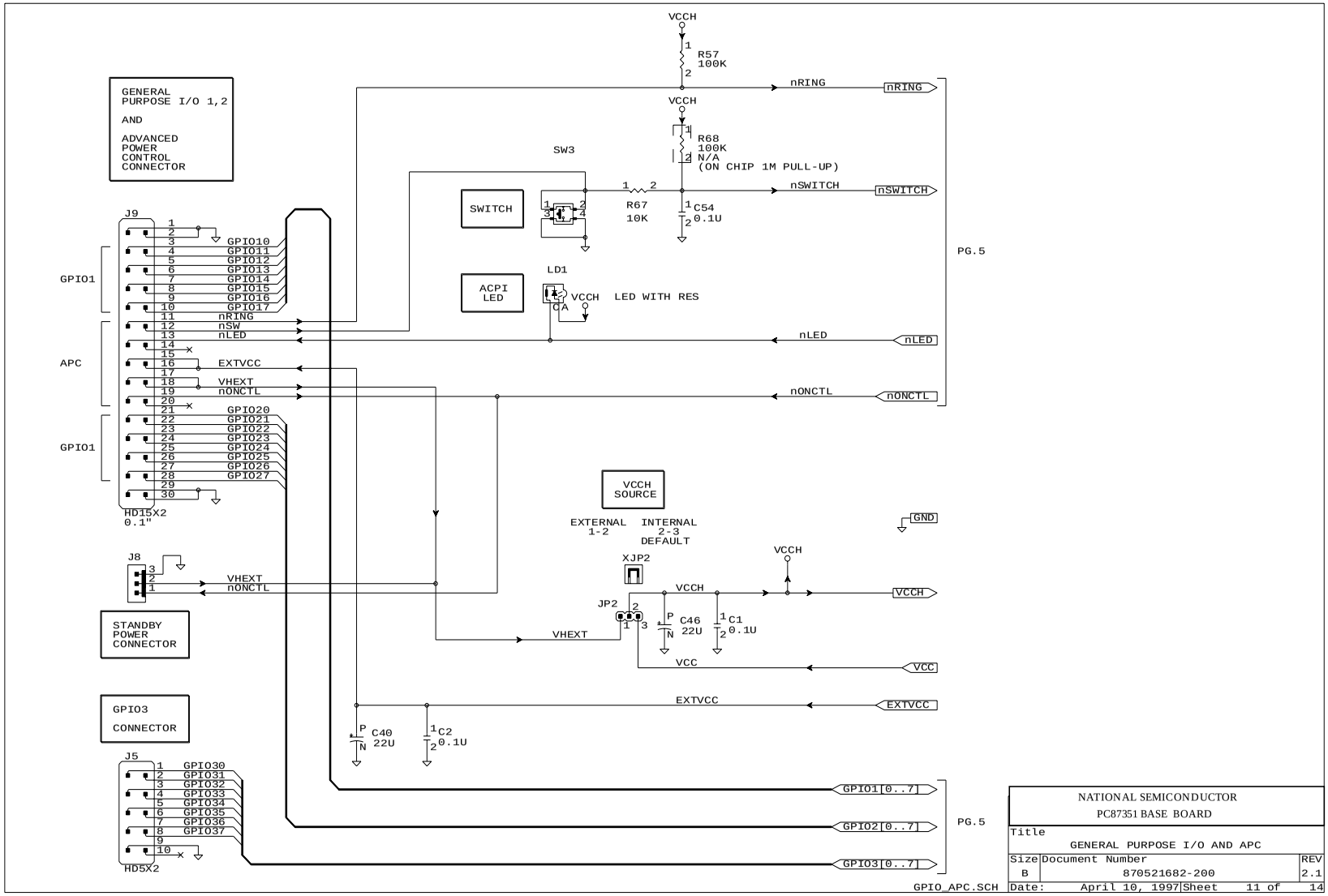


IR MULTIPLEXED SIGNALS		
IRTX		
IRRX1		
IRRX2	IRSL0	ID0
	IRSL1	ID1
	IRSL2	ID2
		ID3

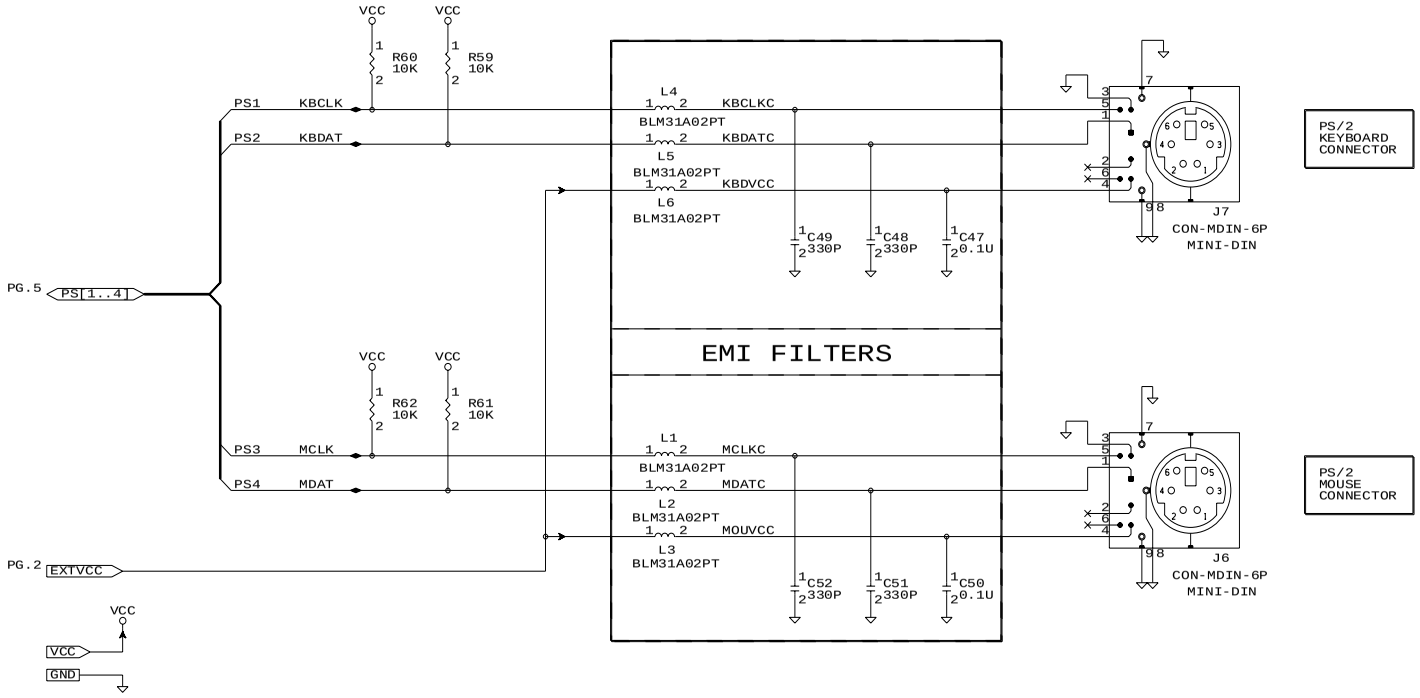
NATIONAL SEMICONDUCTOR PC87351 BASE BOARD		
Title INFRARED PORT CONNECTOR		
Size B	Document Number 870521682-200	REV 2.1
Date: April 10, 1997	Sheet 9 of 14	

IR.SCH


PD[0..7]
PG.5
nSTB
nAFD
nERR
nINIT
nSLIN
nACK
BUSY
PE
SLCT
VCC
R42 4.7K
C6 330P
R43 4.7K
C7 330P
R44 4.7K
C8 330P
R45 4.7K
C9 330P
R46 4.7K
R47 4.7K
C10 330P
R48 4.7K
C11 330P
R49 4.7K
C12 330P
R50 4.7K
C13 330P
R51 4.7K
C14 330P
R52 4.7K
C15 330P
R53 4.7K
C16 330P
R54 4.7K
C17 680P
R55 4.7K
C18 680P
R56 4.7K
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
R19 33R
R20 33R
R21 33R
R22 33R
R23 33R
R24 33R
R25 33R
R26 33R
R27 33R
R28 33R
R29 33R
R30 100R
R31 100R
nRSTB
nRAFD
RPD0
RPD1
RPD2
RPD3
RPD4
RPD5
RPD6
RPD7
nERR
nINIT
nRSLIN
nRACK
RBUSY
PE
SLCT
PARALLEL PORT
J13
CON DB25 FEMALE
SHIELD
PG.6
R81
PCB SHORT
N/A
GND
NATIONAL SEMICONDUCTOR
PC87351 BASE BOARD
Title
PARALLEL PORT TERMINATIONS AND CONNECTOR
Size B
Document Number 870521682-200
REV 2.1
Date: April 10, 1997
Sheet 10 of 14
PAR.SCH



NATIONAL SEMICONDUCTOR PC87351 BASE BOARD		
Title GENERAL PURPOSE I/O AND APC		
Size B	Document Number 870521682-200	REV 2.1
Date: April 10, 1997	Sheet 11 of 14	



NATIONAL SEMICONDUCTOR PC87351 BASE BOARD		
Title PS/2 CONNECTORS		
Size B	Document Number 870521682-200	REV 2.1
Date: April 10, 1997	Sheet 12 of 14	

PS2.SCH

RTC CONNECTOR

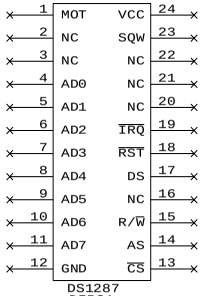
THIS CONNECTOR IS NEEDED FOR EVALUATION PURPOSES ONLY.

CONNECT IT TO THE 24-PIN DIP SOCKET ON THE MOTHERBOARD'S REAL-TIME CLOCK CHIP.

PROCEED AS FOLLOWS :

1. REMOVE THE ORIGINAL DS1287 CHIP (OR EQUIVALENT) AND REPLACE IT WITH A 24-PIN DIP SOCKET.
2. CONNECT J3 TO THE ABOVE SOCKET USING THE SUPPLIED CABLE.
3. PIN 1 (BROWN COLOR) OF THE CABLE MUST BE CONNECTED TO PIN 1 OF J3 AND PIN 1 OF THE SOCKET.

RTC IC PINOUT



DS1287 / MC146818
RTC PINOUT

KBD CONNECTOR

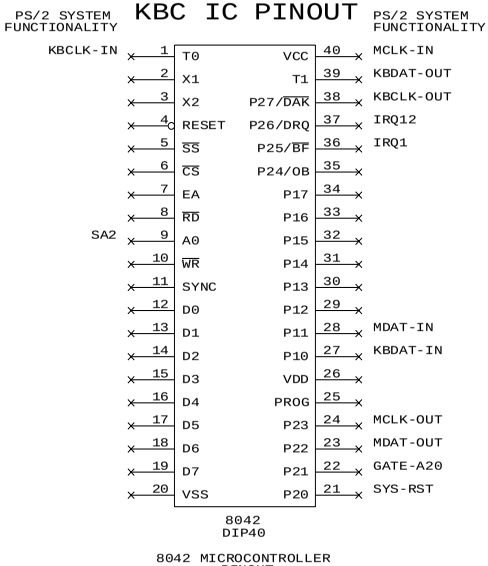
THIS CONNECTOR IS NEEDED FOR EVALUATION PURPOSES ONLY.

CONNECT IT TO THE 40-PIN DIP SOCKET ON THE MOTHERBOARD'S KEYBOARD CONTROLLER CHIP.

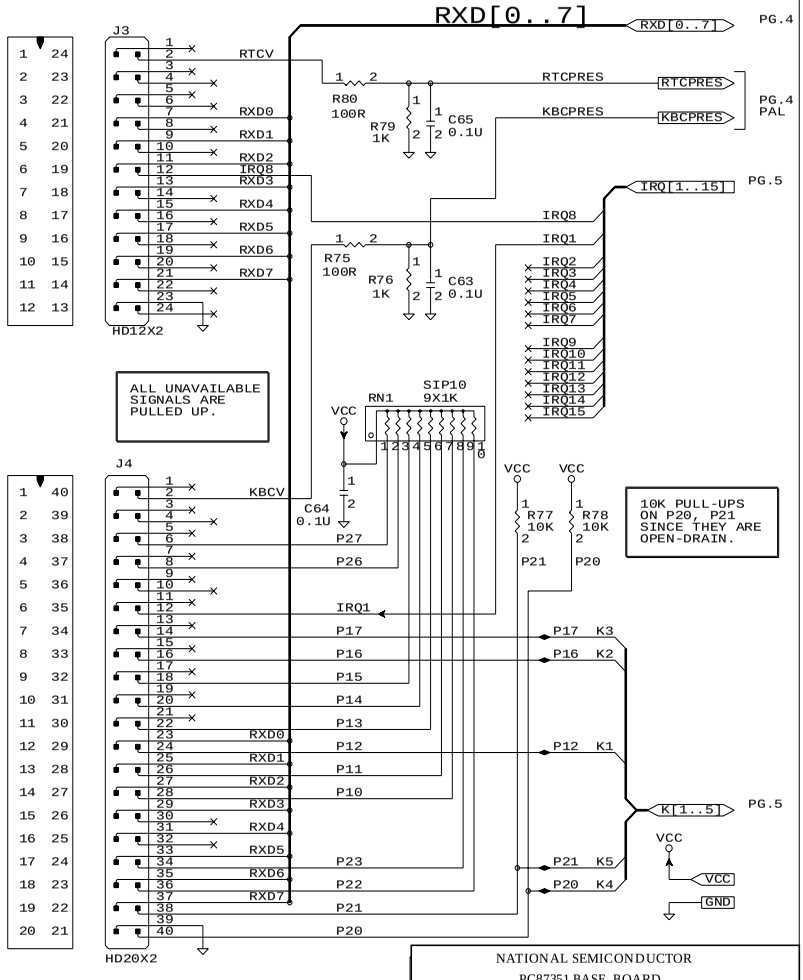
PROCEED AS FOLLOWS :

1. REMOVE THE ORIGINAL 8042 CHIP (OR EQUIVALENT) AND REPLACE IT WITH A 40-PIN DIP SOCKET.
2. CONNECT J4 TO THE ABOVE SOCKET USING THE SUPPLIED CABLE.
3. PIN 1 (BROWN COLOR) OF THE CABLE MUST BE CONNECTED TO PIN 1 OF J4 AND PIN 1 OF THE SOCKET.

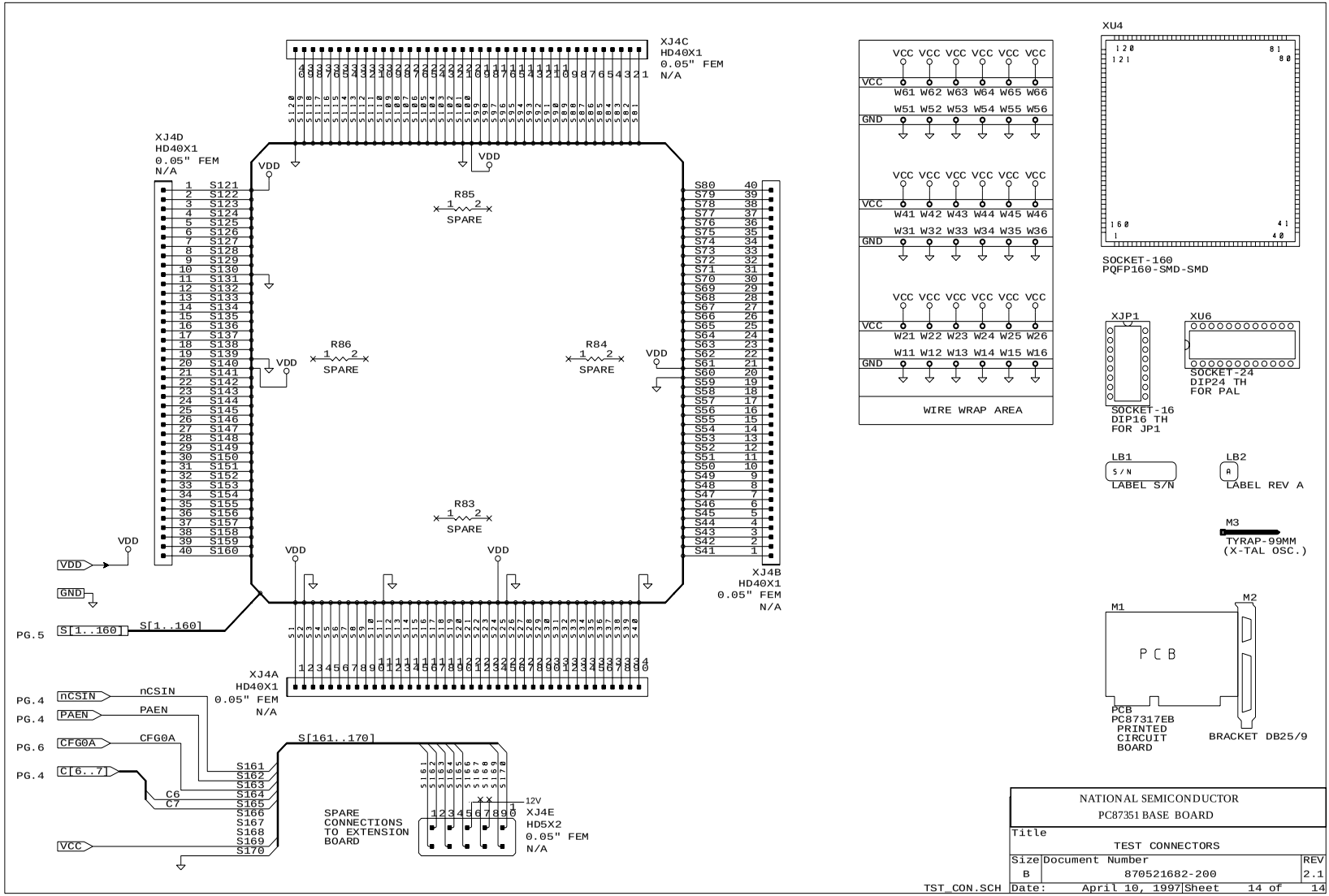
KBC IC PINOUT



8042 MICROCONTROLLER
PINOUT



NATIONAL SEMICONDUCTOR PC87351 BASE BOARD	
Title KBC AND RTC CONNECTORS	
Size B	Document Number 870521682-200 REV 2.1
KBC_RTC.SCH	Date: April 10, 1997 Sheet 13 of 14



NATIONAL SEMICONDUCTOR PC87351 BASE BOARD		
Title TEST CONNECTORS		
Size B	Document Number 870521682-200	REV 2.1
Date: April 10, 1997	Sheet 14 of 14	

TST_CON.SCH

Appendix B
EXTENSION BOARD SCHEMATIC DIAGRAMS

The following pages contain the schematics diagrams for the PC87351EB extension board.

REVISIONS

ECN#	PCB 551521	ASS 980521	SCH	DESCRIPTION	DATE	APPROVED
			1.0	INITIAL VERSION	25 FEB 1998	Y. MARGALIT
	694-001/A	694-001/A	1.1	RELEASED VERSION AFTER BACK ANOTATION	4 MAR 1998	Y. MARGALIT

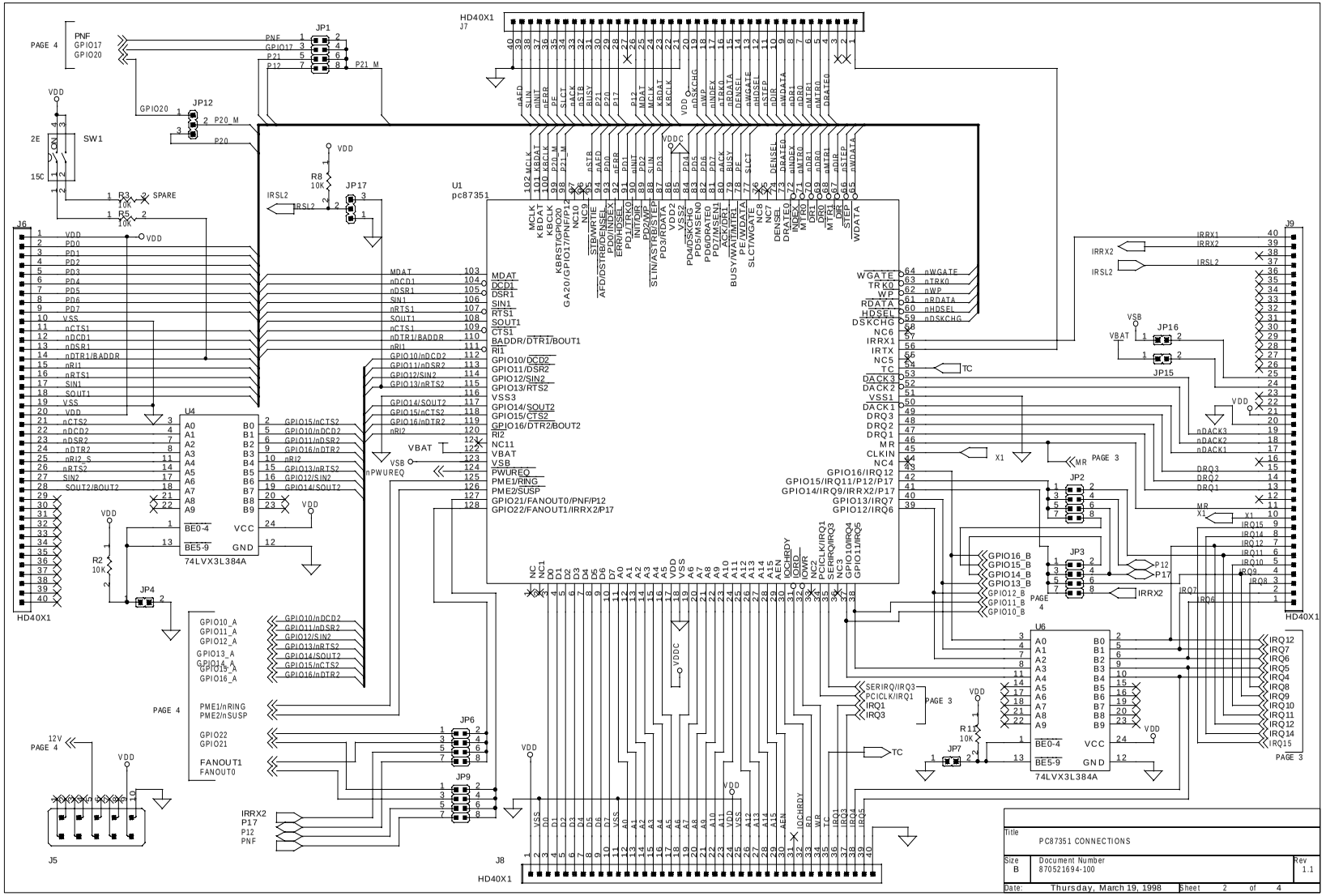
DESIGN FILES (ORCAD)

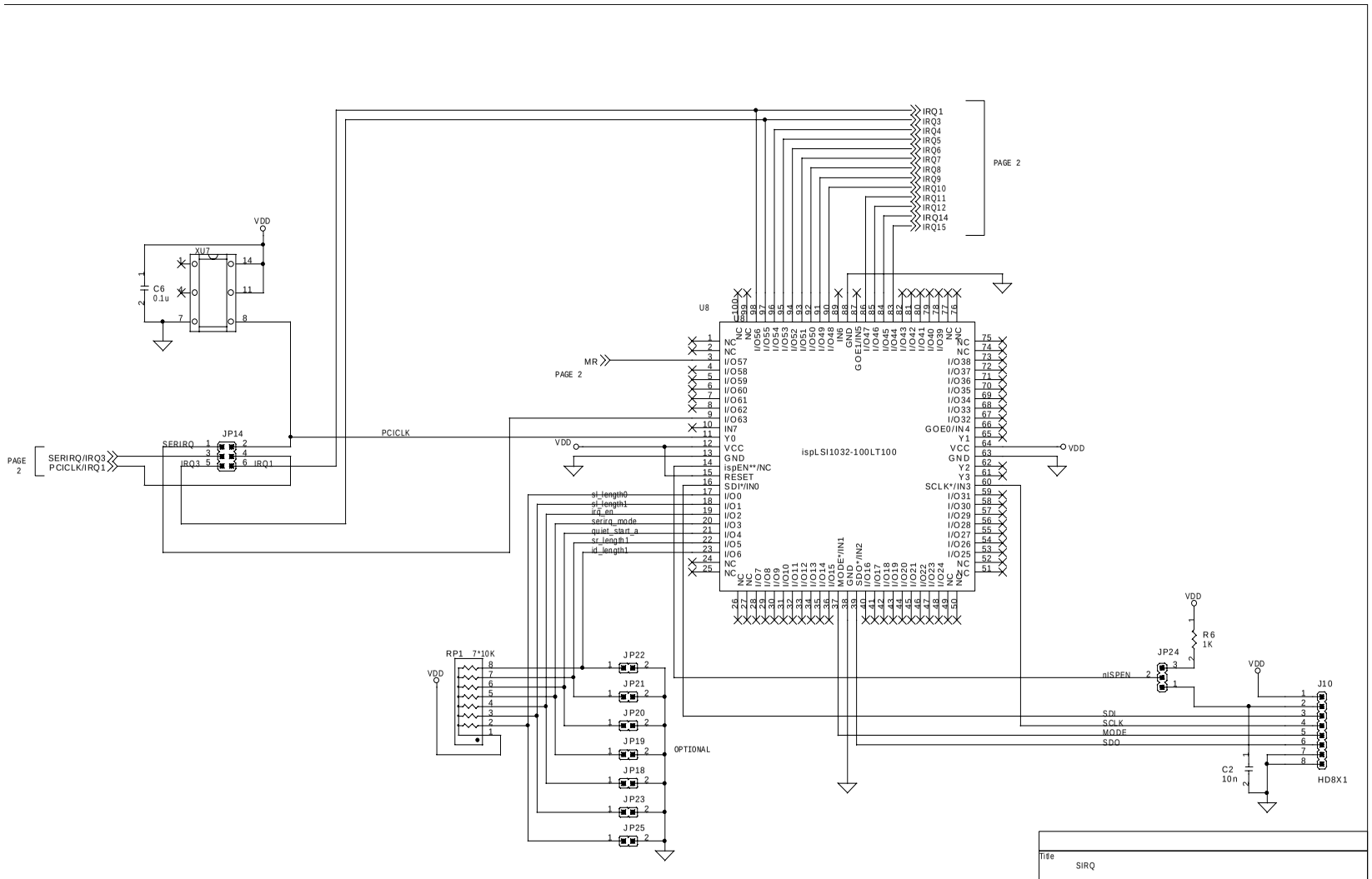
SCHEMATIC:	COVER	PG. 1	COVER PAGE
	PC87351 CONNECTIONS	PG. 2	PC87351 CHIP CONNECTIONS AND GLUE LOGIC
	SIRQ	PG. 3	SERIAL IRQ CIRCUIT
	FAN_PARTS	PG. 4	FAN CIRCUIT AND PARTS
LIBRARY:	NSC1.LIB		NATIONAL SEMICONDUCTOR LIBRARY

PC87351

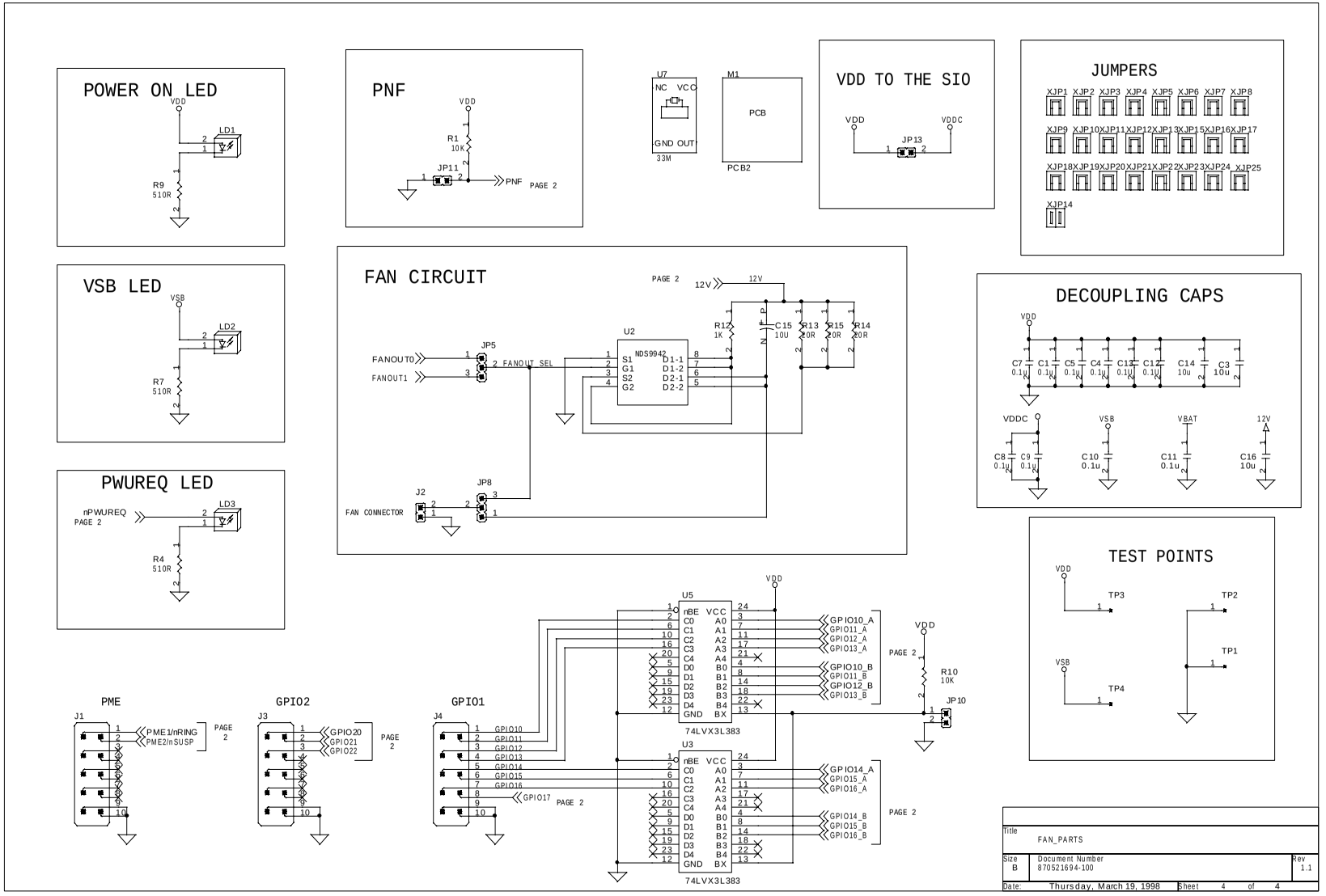
EXTENSION BOARD

Title	COVER PAGE	
Size B	Document Number 870521694-100	Rev 1.1
Date: Thursday, March 19, 1998	Sheet 1 of 4	


U1
pc87351
HD40X1
J7
J8
J6
J9
J5
U4
U6
74LVX3L384A
JP1
JP12
JP17
JP16
JP15
JP2
JP3
JP4
JP6
JP7
JP9
SW1
R3
R5
R8
R11
R2
SPARE
PAGE 4
PAGE 3
Title
PC87351 CONNECTIONS
Size
B
Document Number
870521694-100
Rev
1.1
Date:
Thursday, March 19, 1998
Sheet
2
of
4



Title	SIRQ		
Size B	Document Number 870521694-100		Rev 1.1
Date: Thursday, April 09, 1998	Sheet 3 of 4		


POWER ON LED
VDD
LD1
R9
510R
PNF
VDD
R1
10K
JP11
PNF
PAGE 2
U7
NC
VCC
GND
OUT
33M
M1
PCB
PCB2
VDD TO THE SIO
VDD
VDDC
JP13
JUMPERS
XJP1 XJP2 XJP3 XJP4 XJP5 XJP6 XJP7 XJP8
XJP9 XJP10 XJP11 XJP12 XJP13 XJP15 XJP16 XJP17
XJP18 XJP19 XJP20 XJP21 XJP22 XJP23 XJP24 XJP25
XJP14
VSB LED
VSB
LD2
R7
510R
FAN CIRCUIT
PAGE 2
12V
12V
R12
1K
C15
10U
R13
20R
R15
20R
R14
20R
U2
NDS9942
S1
G1
S2
G2
D1-1
D1-2
D2-1
D2-2
FANOUT0
FANOUT1
JP5
FANOUT_SEL
J2
JP8
FAN CONNECTOR
DECOUPLING CAPS
VDD
C7
0.1u
C1
0.1u
C5
0.1u
C4
0.1u
C13
0.1u
C12
0.1u
C14
10u
C3
10u
VDDC
VSB
VBAT
12V
C8
0.1u
C9
0.1u
C10
0.1u
C11
0.1u
C16
10u
PWUREQ LED
nPWUREQ
PAGE 2
LD3
R4
510R
TEST POINTS
VDD
TP3
TP2
TP1
VSB
TP4
U5
nBE
VCC
C0
C1
C2
C3
C4
D0
D1
D2
D3
D4
GND
A0
A1
A2
A3
A4
B0
B1
B2
B3
B4
BX
74LVX3L383
GPIO10_A
GPIO11_A
GPIO12_A
GPIO13_A
GPIO10_B
GPIO11_B
GPIO12_B
GPIO13_B
PAGE 2
VDD
R10
10K
JP10
U3
74LVX3L383
GPIO14_A
GPIO15_A
GPIO16_A
GPIO14_B
GPIO15_B
GPIO16_B
PAGE 2
PME
J1
PME1/nRING
PME2/nSUSP
PAGE 2
GPIO2
J3
GPIO20
GPIO21
GPIO22
PAGE 2
GPIO1
J4
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
PAGE 2
Title
FAN_PARTS
Size
B
Document Number
870521694-100
Rev
1.1
Date:
Thursday, March 19, 1998
Sheet
4
of
4

Appendix C
BILL OF MATERIALS

Description	Location	Qty
Base Board		
74LVX3L384A SMD-TSOP24 BUS SWITCH 3 OR 5V	U10, U5	2
PAL22V10 DIP24 7.5NS, 0.3"	U6	1
74ACTQ32 SMD-SO14S QUAD OR GATES	U7	1
74ACT00 SMD-SO14S QUAD NAND GATES	U8	1
DS14185M SMD-SO20W +/-12, +5V UART DRV/RCV	U1, U2	2
DS14C89A SMD-SO14S +5V UART RECEIVER	U3	1
33R SMD-1206 1/4W 5%	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R34	28
100R SMD-1206 1/4W 5%	R30, R31, R58, R75	4
1K SMD-1206 1/4W 5%	R76	1
4.7K SMD-1206 1/4W 5%	R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56	15
10K SMD-1206 1/4W 5%	R32, R33, R59, R60, R61, R62, R77, R78	8
10K DIP 1/4W 5%	R41	1
150K SMD-1206 1/4W 5%	R35, R36, R37, R38, R39	5
SPARE SMD-1206 1/4W SPARE FOOTPRINT	R82, R83, R84, R85, R86	5
RES-NET-COM-9 SIP10 9X1K SIP10, 2%, 1/8W	RN1	1
RES-NET-COM-5 SIP6 5X1K SIP6, 5%, 1/8W	RN2	1
RES-NET-ISOL-8 DIP16 8X10R DIP16, 0.3”, 1%, 1/8W	JP1	1
47P SMD-0805 50V C-NP, CER NPO, 10%,	C33	1
200P SMD-0805 50V C-NP, CER NPO, 10%	C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81	16
330P SMD-0805 50V C-NP, CER NPO, 10%	C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C48, C49, C51, C52	15
680P SMD-0805 50V C-NP, CER NPO, 10%	C17, C18	2

Description	Location	Qty
0.1U SMD-1206 50V C-NP, CER X7R, 10%	C1, C2, C19, C21, C22, C23, C24, C26, C28, C30, C31, C32, C34, C36, C37, C38, C39, C41, C43, C44, C47, C50, C55, C56, C57, C59, C60, C61, C62, C63, C64	31
22U SMD-6032 16V C-POL, TANT, 10%	C25, C27, C29, C35, C40, C42, C45, C46, C58	9
BLM31A02PT SMD-1206 200mA INDUCTOR, EMI BEAD	L1, L2, L3, L4, L5, L6	6
CRYSTAL-OSC DIP14 48MHz 100PPM, CMOS, 5V	U9	1
CON-MDIN-6P MINI-DIN 6 PINS + 3 SHIELD PINS	J7, J6	2
CON DB9 FEMALE TH-RA PCB	J12	1
CON DB25 FEMALE TH-RA PCB	J13	1
CON 3 PIN POL 2.5MM HD LOCK POLARIZED	J8	1
HD1X1 0.1” HEADER, 1 PIN	TP2, TP3	2
HD2X1 0.1” HEADER, 2 PINS	JP4	1
JUMPER-COVER-2PIN, BLACK	XJP2, XJP4	2
HD3X1 0.1” HEADER, 3 PINS	JP2	1
HD40X1 0.05” FEM HEADER, 40 PINS	XJ4D, XJ4C, XJ4B, XJ4A	4
HD5X2 0.1” SHROUDED HEADER, 10 PINS	J1, J2	2
HD17X2 0.1” SHROUDED HEADER, 34 PINS	J10	1
HD20X2 0.1” SHROUDED HEADER, 40 PINS	J4	1
HD5X2 FEM HD 0.05”X0.1”	XJ4E	1
SOCKET-24 DIP24, O.3”	XU6	1
SW-SPDT-MOM 0.1” 5P 2 SHIELD PINS	SW4	1
FUSE-SOCKET SMD 2A SOCKET + FUSE SLOW BLOW	XF1	1
BATT-3PIN COIN 3.0V LITHIUM CELL 380mAH	BT1	1
PCB PC87317EB PRINTED CIRCUIT BOARD	M1	1
BRACKET DB25/9 IBM PC-AT	M2	1
LABEL REV A REV LET ‘A’	LB2	1
LABEL S/N	LB1	1
Extension Board		
PC87351-XXX/ SMD-PQFP128 SUPERI/O	U1	1
SI9942 DUAL MOSFET	U2	1
CRYSTAL-OSC DIP14 33MHz 50PPM, TTL, 5V	U7	1
74LVX3L383 SMD-TSOP24 BUS CHANGER 3 OR 5V	U3, U5	2

Description	Location	Qty
74LVX3L384A SMD-TSOP24 BUS SWITCH 3 OR 5V	U4, U6	2
ispLSI1032E-100LT CPLD	U8	1
SW-DP-NO-NC-X2 DIP4 DIPSWITCHX2	SW1	1
SOCKET-OSC 14/6 DIP14 6PINS ROUND	XU7	1
HD3X1 0.1” HEADER, 3 PINS	JP5, JP8, JP12, JP17, JP24	5
HD8X1 0.1” HEADER, 8 PINS	J10	1
HD2X1 0.1” HEADER, 2 PINS	J2, JP4, JP7, JP10, JP11, JP13, JP15, JP16, JP18, JP19, JP20, JP21, GP22, JP23, JP25	15
HD5X2 0.1” SHROUDED HEADER, 10 PINS	J1, J2, J3	3
HD3X2 0.1” SHROUDED HEADER, 6 PINS	JP14	1
HD4X2 0.1” SHROUDED HEADER, 8 PINS	JP1, JP2, JP3, JP6, JP9	5
HD5X2 FEM HD 0.05”X0.1”	J5	1
HD40X1 0.05” MALE	J7, J8, J9	3
HD30X1 0.05” MALE	J6	1
HD1X1 0.1” HEADER, 1 PIN	TP1, TP2, TP3, TP4	4
JUMPER-COVER-2PIN, BLACK	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7, XJP8, XJP9, XJP10, XJP11, XJP12, XJP13, XJP15, XJP16, XJP17, XJP18, XJP19, XJP20, XJP21, XJP22, XJP23, XJP24, XJP25	24
JUMPER-COVER-2PIN-X2, BLACK	XJP14	1
SOCKET-128 PQFP128-SMD-SMD	XU1	1
10K SMD-1206 1/4W 5%	R1, R2, R3, R5, R8, R10, R11	7
510R SMD-1206 1/4W 5%	R4, R7, R9	3
20R SMD-1206 1/4W 5%	R13, R14, R15	3
1K SMD-1206 1/4W 5%	R6, R12	2
RES-NET-COM-7 SIP8 7X1K SIP8, 2%, 1/8W	RP1	1
0.1U SMD-0805 50V C-NP, CER X7R, 10%	C1, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13	11
10n SMD-0805 50V C-NP, CER X7R, 10%	C2	1
10U SMD-6032 20V C-NP, 10%	C3, C14, C15, C16	
LABEL REV A REV LET ‘A’	LB1	1
RED LED SQUARE	LD1, LD2, LD3	3

Appendix D
PAL EQUATIONS

The PAL equations of the PC87351EB PLD - XU6:

```
"*************************************************************************
"*        NATIONAL        SEMICONDUCTOR          CORPORATION             *
"*                                                                       *
"*                                                                       *
"*        Revision   Date              Description                      *
"*        ------------------------------------------------               *
"*         0.1        Feb 21, 1997    PC87351EB EVALUATION BOARD        *
"*        Author: Theodor Iacob                                          *
"*************************************************************************

module M351EB

title '351EB XBUS/ISA buffer control logic '

M351EBdevice'P22V10';

declarations

"INPUTS
"======

SA0,SA1,SA2,SA3,SA4,SA5 pin 1,2,3,4,5,6;
SA6,SA7,SA8,SA9,SA10,SA11 pin 7,8,9,10,11,13;
NCSIN                 pin 17;" NCSIN = SA15 # SA14 # SA13 # SA12
                           " delivered by external logic
AEN                   pin 16;
NIORD                 pin 15;
NIOWR                 pin 14;
CFG0A                 pin 21;
KBCPRES               pin 22;
RTCPRES               pin 23;

"OUTPUTS
"=======
NISAENBL              pin 20;
NXENBL                pin 19;
PAEN                  pin 18;

ADDR12     = [SA11,SA10,SA9,SA8,SA7,SA6,SA5,SA4,SA3,SA2,SA1,SA0];
ADDR11     =        [SA10,SA9,SA8,SA7,SA6,SA5,SA4,SA3,SA2,SA1,SA0];

KBC_ACCESS= !NCSIN & (( ADDR12 == ^h060 ) # ( ADDR12 == ^h064 ));
RTC_ACCESS= !NCSIN & (( ADDR12 == ^h070 ) # ( ADDR12 == ^h071 ));

H,L,X,C    = 1, 0 , .X. , .C.;
```

```
equations

!NXENBL    = (( KBCPRES & KBC_ACCESS ) #“KBC cable connected AND
                                “KBC address match OR
               ( RTCPRES & RTC_ACCESS ) “RTC cable connected AND
             ) &               “RTC address match OR
            !AEN &        “AEN must be low AND
            (!NIORD # !NIOWR ); “read OR write cycle

!NISAENBL= (!NIORD # !NIOWR ) &             “read or write cycle AND
              (AEN #                          “ for DMA cycles: AEN is High
                                “    AND any addr. OR
                                “ for IO  cycles:
               (!AEN &    “AEN is LOW AND
                (!KBC_ACCESS &      “there is not a KBC access AND
                           !RTC_ACCESS“there is not a RTC access.
                         )
                       )
                     );
```

INDEX

M

P

R

S

T

U

National Semiconductor supplies a comprehensive set of service and support capabilities. Complete product information and design support is available from National's customer support centers.

To receive sales literature and technical assistance, contact the National support center in your area.

Americas	**Fax:**	**1-800-737-7018**
	Email:	**support@nsc.com**
	Tel:	**1-800-272-9959**
Europe	**Fax:**	**+49 (0)1 80 5 30 85 86**
	Email:	**europe.support@nsc.com**
Deutsch	**Tel:**	**+49 (0)1 80 5 30 85 85**
English	**Tel:**	**+49 (0)1 80 5 32 78 32**
Japan	**Fax:**	**81-3-5620-6179**
	Tel:	**81-3-5620-6175**
Southeast Asia	**Fax:**	**65-250-4466**
	Email:	**sea.support@nsc.com**
	Tel:	**65-254-4466**

Visit us on the Worldwide Web at: http://www.national.com